

Pre-Bonding Flip-Chip Process and Reliability Assessment

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Abstract

This paper has evaluated 2 types of flip chip assembly process technology: the conventional process and the Pre-Bonding process. The Pre-Bonding process has the advantages of less process steps, higher aesthetic finishing, and more compatible to surface mount technology. These advantages would make flip chip as a viable product consideration. 3 types of packages were used to illustrate the manufacturability and reliability of Pre-Bonding Technology. Package A is a flip chip BGA with more than 400 I/O, Package B is a flip chip on ceramic with 180 I/O and Package C is another flip chip BGA with 120 I/O. Whether it is manufacturing in singular form or in array format, Pre-Bonding flip chip has shown its robustness and reliability to be on par with BGA packages.

Introduction

Traditionally, flip chip bonding technology usage had been restricted to large-scale computers as a mean to improve performance. Special chips, expensive substrates and customised equipment were necessary for the assembly process. Application of this costly technology was nearly impossible for the cost sensitive products. However, flip chip has gathered a lot of momentum in recent years, especially within the electronic industry. The advantages of flip chip are just too great to ignore. Among those are, minimum parasitic values which improve high-speed performance, low profile and small footprint that enable product miniaturisation, and compatibility to the surface mount assembly which is the current industry mainstream.

In order to make the flip chip technology viable to all products, several critical problems must be solved before wide scale application is feasible. One of the current limitations is the full compatibility with surface mount technology (SMT). To do that, solder based flip chip assembly on organic substrate is required. However, such assembly configuration needs an epoxy material to underfill between the chip and the substrate in order to improve the reliability.

The time required for dispensing the underfill and subject to the capillary effect of the material flow, is not compatible to SMT. Furthermore, after underfill application, the resin must be cured in an oven (Figure 1). All these additional processes make flip chip unattractive.

In view of the incompatibility of the flip chip process, it is therefore a need to find an alternative method of manufacturing. The technology and materials discussed in this paper, referred to as Pre-Bonding Flip Chip, provide an alternative flip chip assembly method which eliminates the need for a separate underfill operation.

Test Vehicles

3 types of chips and 2 types of substrate were selected as the test vehicles. These test chips were selected based on bump configuration, pitch size, number of I/O and substrate materials. Chip 1 is a daisy-chained chip with 416 I/O in array format and 200 μm pitch; Chip 2 is also a daisy-chained chip with 180 peripheral I/O and 200 μm pitch; Chip 3 is a daisy-chained chip with 120 peripheral I/O and 300 μm pitch. The three chips details are shown in Table 1.

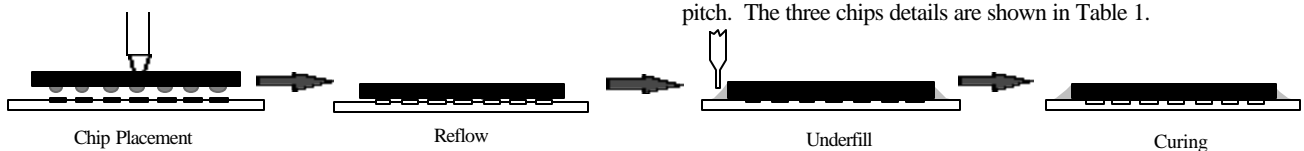


Figure 1 Conventional flip chip assembly process [1,2]

Table 1 Details of Test Vehicles

	Chip 1	Chip 2	Chip 3
Chip size (mm)	9 x 9	10 x 10	10 x 10
# of I/O	416	180	120
Configuration	Array	Peripheral	Peripheral
Bump pitch	200 μ m	200 μ m	300 μ m
Bump height	90 μ m	90 μ m	90 μ m
Bump Mat'l	63/37	63/37	63/37

Table 2 gives details of the various substrates. Substrate pads on the chip sites were designed to match the chip pad dimensions. The surface finishes of organic boards are nickel plated with flash gold, while plated solder finishing is used for the ceramic board.

Table 2 Details of Substrates

	Subst. 1	Subst. 2	Subst. 3
Board size (mm)	220 x 60 (12 x 12)	33 x 33	25 x 25
Units/Board	64	1	1
Material	Organic	Ceramic	Organic
Surface finish	Ni/Au	Pb/Sn	Ni/Au
Board thick's	0.36 mm	1.00 mm	0.36 mm
Line/Space width	76/76 μ m	76/76 μ m	50/76 μ m

3 types of packages were assembled using the Pre-Bonding flip chip technique described here. The chips and substrates were described in the previous section on Test Vehicles. Package A consists of Chip 1 and Substrate 1 (Figure 3) is actually diced from a strip of 64 units. Package B consists of Chip 2 and Substrate 2 (Figure 4) is a ceramic package with test pads at the peripheral. Package C consists of Chip 3 and Substrate 3 is a BT package with test pads at the corners. The test pads of Packages B and C will facilitate the chain resistance measurement. Electrical measurement for Package A could only be done on the solder ball side of the package.

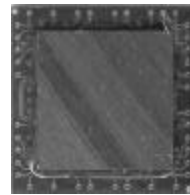


Figure 3 Package A

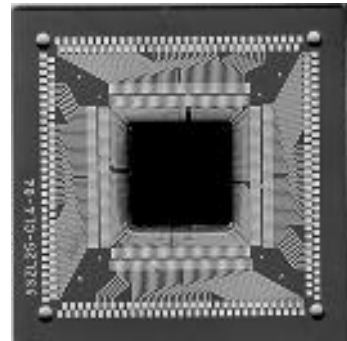


Figure 4 Package B

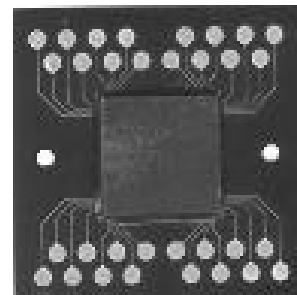


Figure 5 Package C

Pre-Bonding FC Assembly Process

An alternative method of flip chip technology (Figure 2) is proposed here as the Pre-Bonding flip chip process. Pre-Bonding is a 3step process. First of all, the “underfill” material is dispensed. After which, a chip can be placed immediately onto the substrate. The placement action would thus cause the “underfill” material to spread under compression flow. Compression flow is almost completed instantaneously. Therefore, the substrate can be subjected to the in-line solder reflow process. Pre-Bonding has eliminated the necessity of underfilling. Incidentally, we also named the “underfill” material as P-Bond.

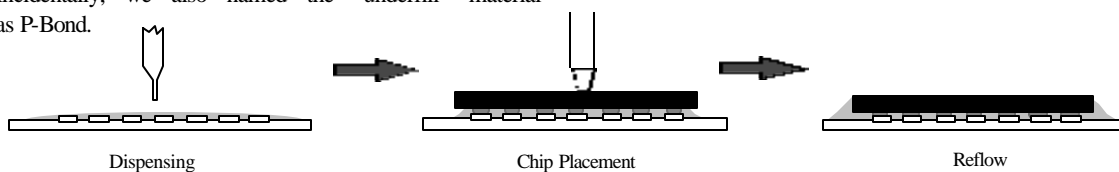


Figure 2 Pre-Bonding Flip Chip Assembly Process

In a typical Pre-Bonding Flip Chip process, the dispensing of the P-Bond epoxy is easily done with an X-pattern. The ease of dispensing was more obvious on a larger board format such as Substrate 1. The whole board can accommodate 64 units, with 16 units on each of the four panel (Figure 6). Figures 6 and 7 compare the epoxy dispensing method of Pre-Bonding flip chip and conventional flip chip. The Pre-Bonding method showed equal fillet shape on all sides of the package. On the other hand, the conventional method showed a bigger trace of dispensing on one side of the package. As a result, larger unit size would be required. Hence, it would be more difficult to build Chip Scale Packages with conventional flip chip method.

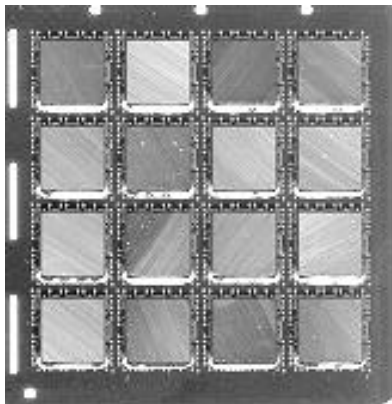


Figure 6 Pre-Bonding FC

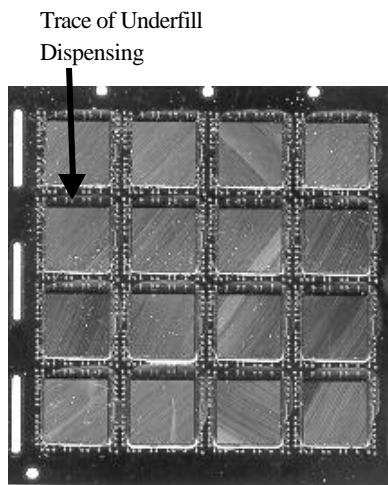


Figure 7 Conventional FC

Characterisation

To characterise the stability of interconnect, electrical resistance measurements were performed on the packages. Figures 8 - 10 present the histograms of the initial chain resistance measured for the samples. The

mean values of the chain resistance for Packages A, B and C are 22, 11 and 0.5 ohm respectively.

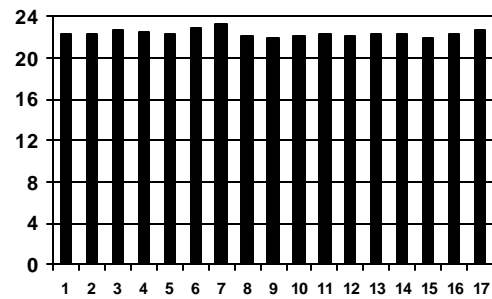


Figure 8 Initial resistance measurement for Package A

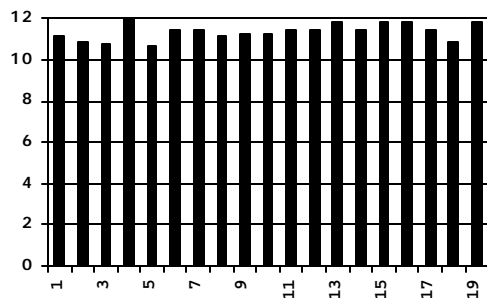


Figure 9 Initial resistance measurement for Package B

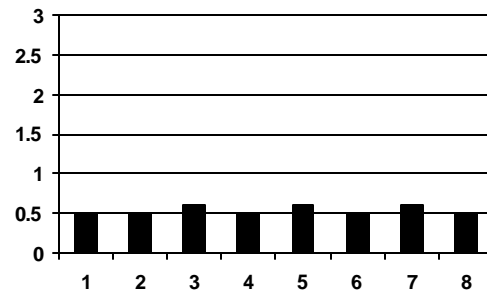


Figure 10 Initial resistance measurement for Package C

Reliability Tests

Package reliability is an integral part in qualifying any new product and/or material. The most common tests conducted in the industry are: moisture sensitivity, temperature humidity, temperature cycling and high temperature storage. The reliability test programs are designed according to the flow charts indicated in Figures 11 and 12.

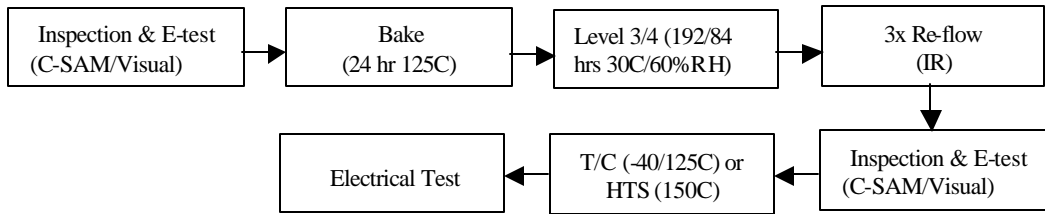


Figure 11 Reliability test program for moisture sensitivity, temp cycle and high temp storage test

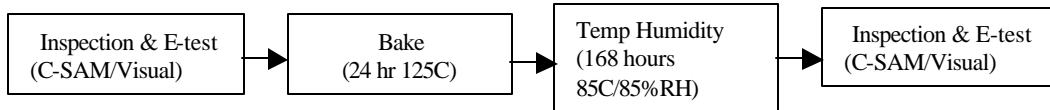


Figure 12 Reliability test program for temperature humidity test

The major concern among all the reliability tests is the moisture sensitivity test where ‘popcorn’ package cracking is an industry wide problem. Therefore, the target set for the reliability standard of the Pre-Bonding flip chip technology is to be comparable, to organic substrate based BGA technology. The failure criteria used in the above reliability programs are visual inspection, delamination check and electrical test. Visual inspection is done with the aid of a microscope set at 40X magnification. Whereas, scanning acoustic microscopy is used to check for delamination in the package. Electrical test is used to measure the (daisy) chain resistance after reliability tests. The package would be considered fail when crack, delamination or resistance change of more than 20% is observed.

Results

In the preliminary testing on moisture sensitivity, all the packages tested did not show any failure (Table 3). A typical scanning acoustic microscopy picture was shown in Figure 13. The figure depicted Package B after Level 4 moisture sensitivity test. Figures 14 ~ 16 showed no significant changes in the chain resistance measurement on the packages.

Table 3 Package Characterisation after Moisture Sensitivity Test

	Package A	Package B	Package C
Visual Insp.	No crack	No crack	No crack
Delamination	No	No	No
Δ in electrical measurement	< 5%	< 10%	< 5%

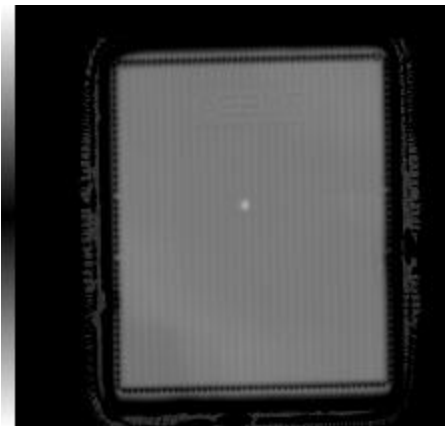


Figure 13 SAM picture of Package B after moisture sensitivity test

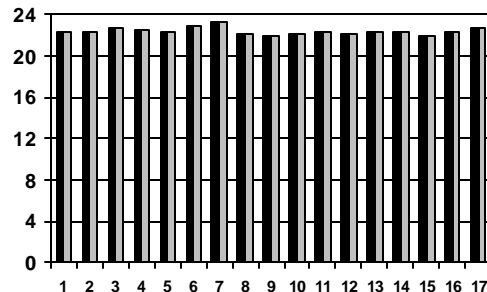


Figure 14 Chain resistance for Package A after Level 3 test

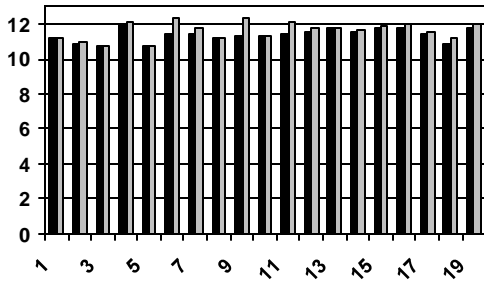


Figure 15 Chain resistance for Package B after Level 4 test

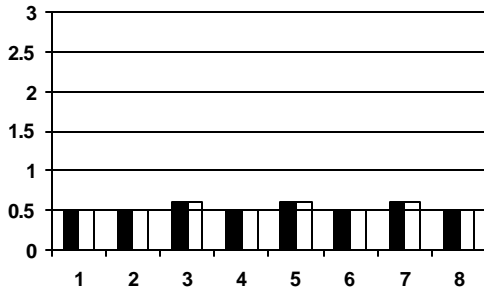


Figure 16 Chain resistance for Package C after Level 3 test

As the packages passed the moisture sensitivity test, we proceeded with a more extensive reliability program as stated in Figures 11 and 12. Table 4 showed the results of the reliability tests. All the packages assembled with Pre-Bonding Flip Chip Technology passed the reliability programs tested.

Table 4 Package Reliability Characterisation

	Package A	Package B	Package C
Moisture Pre-conditioning	Pass Level 3	Pass Level 4	Pass Level 3
Moisture Pre-Cond. + T/C	Test in progress	Pass 1500 cycles	Pass 2000 cycles
Moisture Pre-Cond. + HTS	Test in progress	Pass 1000 hours	-
Δ in electrical measurement after 85C/85%RH	Test in progress	-	-

Discussion

The P-Bond material developed for this project was a result of an extensive study of material characteristic, “reflowable” property, manufacturability and reliability.

Differential scanning calorimetry, DSC (Figure 17) and thermomechanical analysis, TMA (Figure 18) were performed to determine the exotherm initiation temperature (EIT) and glass transition temperature (Tg) respectively, of P-Bond and the conventional underfill.

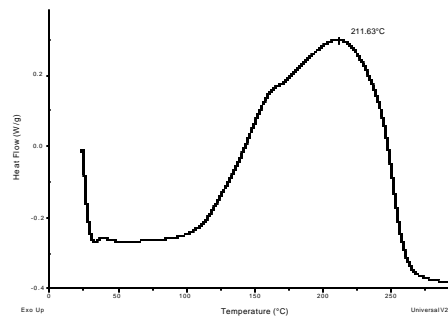


Figure 17 DSC test on P-Bond

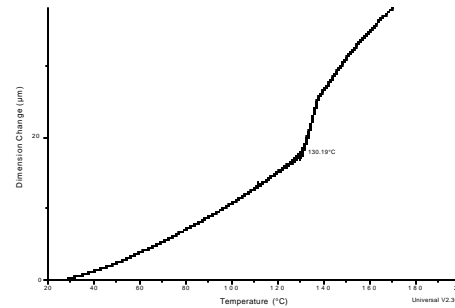


Figure 18 TMA test on P-Bond

Table 5 DSC and TMA Characterisation

Material	EIT (°C)	Tg (°C)
Conventional Underfill	115	150
P-Bond	211	130

In terms of reflow property, the ability to wet the substrate bond pad at 183°C of eutectic solder melting temperature is very critical. Improper wetting will result in dry joint (Figure 19) or no contact (Figure 20).

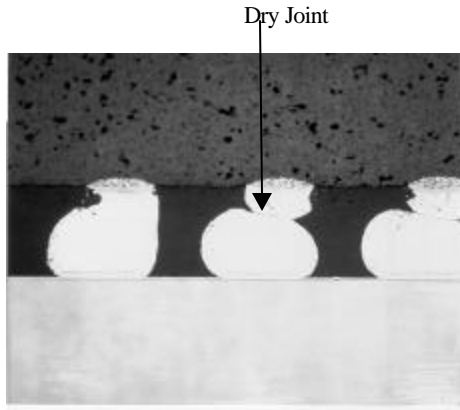


Figure 19 Dry joint after reflow process

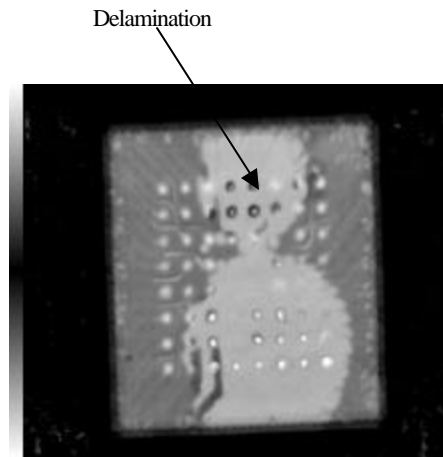


Figure 22 Package Delamination

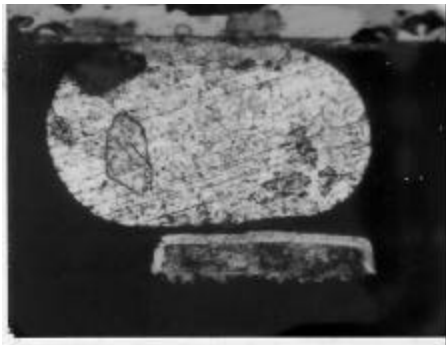


Figure 20 No contact after reflow process

In terms of manufacturability, the material must not generate too much voids during the assembly process. Voids are detrimental as subsequent reflow after moisture pre-conditioning may cause solder balling (Figure 21) or delamination (Figure 22).

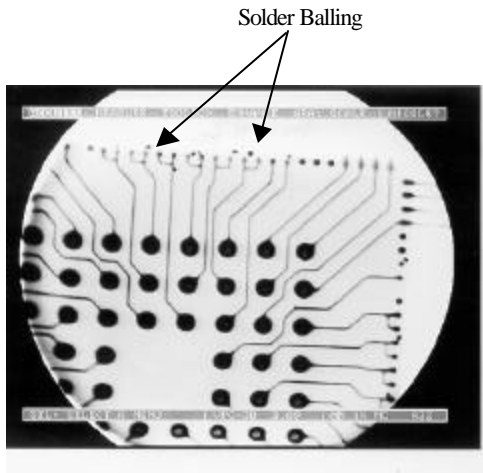


Figure 21 Solder balling after multiple reflow

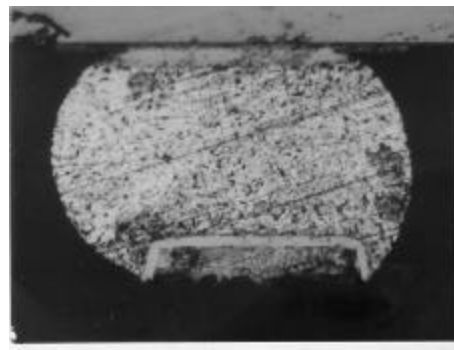


Figure 23 Good joint with P-Bond

With the full understanding of material behaviour, and its correlation to manufacturability and reliability, P-Bond material has been able to demonstrate its capability. The solder joints formed are in perfect contact and good reliability strength (Figure 23). Furthermore, the manufacturing process is in full compliance to the current state of the art, i.e. Surface Mount Technology.

Conclusion

Pre-Bonding flip chip process has been demonstrated as a viable manufacturing process. The beauty of the process is that it is in full compliance with the traditional SMT. Furthermore, the 3 packages assembled with this process had shown excellent package integrity. The process under study in this paper enable a shorter manufacturing cycle time, hence a lower production cost for flip chip technology.

References

[1] Grace O'Malley, Jan Giesler, and Steve Machuga, "The Importance of Material Selection for Flip Chip on Board Assemblies", IEEE Transactions on CPMT Part B, Vol. 17, No. 3, Aug 1994, pp. 248-255.

[2] Sihyun Ha, "Underfill Process Development for SLICC", Proceedings of 1997 Pan Pacific Microelectronics Symposium, pp. 417-420.

Biography

G.L. Tan is the Quality and Reliability Assurance Manager of Questech Solutions, he obtained his B. Eng and M. Eng from the National University of Singapore in 1990 and 1993 respectively. He is presently responsible for the reliability test program in the organization, and to ensure that the products quality are of compliant to the international standard.