Assessment of Flip Chip Assembly and Reliability via Reflowable Underfill

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Abstract

This paper presents process concerns of flip-chip assembly via reflowable underfill in terms of substrate pre-bake, underfill dispensing, chip placement and overmolding that is required in certain applications. Test vehicles with various chip configuration and substrate design have been used in this study. The effects of substrate thickness, bond pad design and solder mask thickness on assembly defects, where void is the major contribution, were extensively elucidated. Meanwhile, approaches to solve the assembly failure have been successfully demonstrated by means of fine-tuning assembly parameters. It was found that voids were mainly from trapped air-bubble during assembly, where underfill dispensing and chip placement are the major sources, rather than from reflowable underfill outgassing during reflow. The trapped voids could become aggravated after solder reflow process. In addition, pad design and solder mask thickness also significantly affect the void level. This study unveils that substrate bond pad with pre-solder on the surface traps less void than those only with nickel/gold finish. For the latter case, substrate heating during underfill dispensing enables to enhance underfill flow and in turn reduces void. Furthermore, die heating that can be implemented via bonding head with heating element during chip placement will dramatically reduce void as well. Discussion will also be given on the impact of solder mask thickness and chip placement speed (search speed) on void, in particularly for non pre-solder capped substrate.

In reliability study, four test vehicles (TV1~TV4) with various specifications have been evaluated, two of which were also overmolded due to drop test requirement from certain devices like mobile phone. JEDEC level 3 moisture preconditioning followed by thermal cycle test (TCT, -55°C ~ 125°C) was performed. Failure analysis was conducted via C-SAM and cross-section. As a result of void, solder extrusion has occurred during TCT that could deteriorate solder bump integrity. Solder crack was also observed from bumps that were isolated from underfill protection arising from void as well. Even under such a condition, fairly good reliability result has been obtained.

Introduction

Flip chip assembly via reflowable underfill is gaining importance and capturing attention of many IC makers and packaging subcontractors because of its simple process flow that has been translated into less machine investment and more efficient production floor utilization. In addition, tedious defluxing and underfilling processes in conventional flip chip assembly are the driving forces for exploring alternatives. Being the integration of underfill and flux function, reflowable underfill possesses self-fluxing capability to make solder reflow and underfilling process occur simultaneously. On the other hand, due to solder bump interconnection yield concern, reflowable underfill is inherently an unfilled/less filled system, no silica filler/minimum filler in formulation with relatively higher coefficient of thermal expansion (CTE, 70~90 ppm/°C). It is well understood that CTE mismatch between silicon chip and organic substrate will cause eutectic solder interconnection failure. Theoretically, underfill with higher CTE value cannot solve CTE mismatch efficiently, which could lead to earlier solder joint failure. Meanwhile, reflowable underfill flow is no longer capillary flow anymore. It started to flow over the bond pad surface after dispensing but changed to compression flow when chip is being placed, which probably generates voids underneath chips. The reliability uncertainty arising from novel reflowable underfill material coupled with new variables from assembly hinders the endorsement of flip chip assembly via reflowable underfill by packaging industry. Therefore, all the concerns have to be resolved before reflowable underfill becomes a real solution. However, few attempts have been made to address the process issues and correlate them with reliability.

The goal of this study is to find out the root cause of generally encountered defects such as void when using reflowable underfill for flip chip assembly. More importantly, solutions for those obstacles have been delivered from both substrate design and assembly process modification approaches.

Experimental

Material

Reflowable underfill used in the present evaluation is P-Bond Ef-7 that was developed in house, and the properties are listed in Table 1.

Table 1. Properties of reflowable underfill

Tg (°C)	CTE (α_1) (ppm/°C)	Modulus @ 25°C (GPa)	Viscosity @25°C (Pa•s)
120~130	70~90	3.2	2.4

Assembly

The schematic process flow for flip chip assembly via reflowable underfill is depicted in Figure 1. Substrates with various bond pad designs were used for assembly process evaluation, such as slot design, pad design, solder mask design and pre-solder deposition, as shown in Figure 2. Substrates were baked at both 125°C and 150°C for different time so that the baking effect could be pronounced. For underfill dispensing study, one drop of underfill was applied onto the top of each substrate, in which both heating and no heating underneath substrate were conducted. Subsequently, chips were placed on the pre-dispensed substrate and the whole

Table 2. Specifications of test vehicle for reliability

		TV1	TV2	TV3	TV4
Chip	Format	Peripheral	Peripheral	Peripheral(3 rounds)	Array
	Die passivation	SiN	SiN	SiN	SiN
	Die size	3 x3 mm	5 x5 mm	10 x10 mm	10 x10 mm
	No. of bumps	36	100	372	1600
	Pitch	250 µm	400 µm	250 µm	250 µm
	Bump material	63Sn/37Pb	63Sn/37Pb	63Sn/37Pb	63Sn/37Pb
Substrate	Type	BT laminate	BT laminate	BT laminate	BT laminate
	Surface finish	Ni/Au	Ni/Au	Ni/Au	Ni/Au
	Pad Design	Slot	Pad define	Slot	Pad define
	Sub. Thickness	0.56mm	0.56mm	0.56mm	1.0mm
	Solder mask thickness	71µm	40µm	81µm	40µm

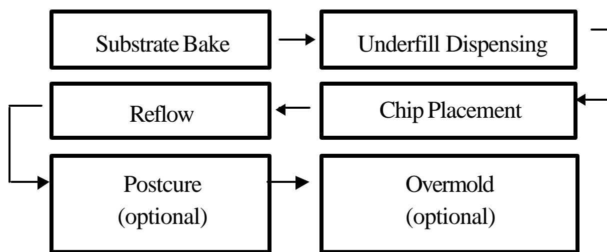


Figure 1. Schematic process flow of flip chip assembly via reflowable underfill

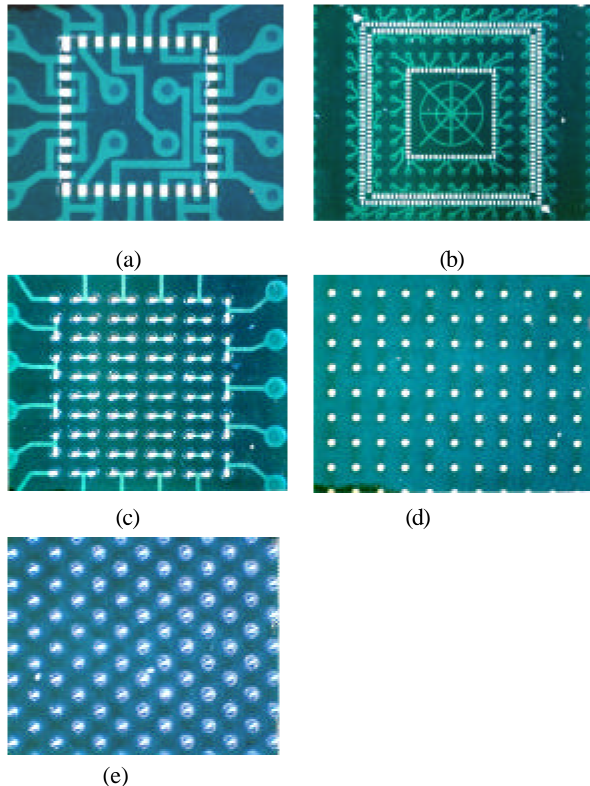


Figure 2. Substrate with various bond pad design (a) slot (b) Slot (3 row) (c) pad define (d) solder mask define (e) pre-solder

assembly was reflowed under a pre-determined reflow profile. Acoustic Scanning Microscopy (C-SAM) was used to detect the void level. In addition, search speed and bonding head heating impact during chip placement were also studied. Lastly, overmolding conditions for flip chip packages was briefly described.

Reliability

Four test vehicles, TV1~TV4, were assembled via optimized process parameters obtained through process evaluation. The specifications of test vehicles were tabulated in Table 2. Part of TV1 and TV2 were overmolded. As such, totally 6 test vehicles were made for reliability evaluation with sample size of 32 units each. JEDEC level 3 moisture sensitivity preconditioning together with three-time oven reflow with peak temperature of 240°C were conducted prior to thermal cycling test (TCT, -55°C ~ 125°C). Unit failure was defined as electrical open circuit. C-SAM with transducer frequency of 100 MHz was used to examine the voids as well as delamination, which were conducted for all the units both before and after reliability.

Results and Discussion

Substrate pre-bake

In general, there are two types of substrates for flip chip packages evaluation. One is double layer that is for low pin count package, usually thin and in matrix form. Another one is multi-layer build-up type that is for high pin count package, normally thick and in singulated form. In the present session, these two type substrates were exemplified by TV1 with thickness of 0.56 mm and one build-up board with thickness of 1.0mm. The substrate pre-bake effect for above two test vehicles was shown in Figure 3 and Figure 4, respectively. It can be seen in Figure 3 that baking at 125°C for 2 h is sufficient to obtain void acceptable TV1 assembly. On the other hand, thick multi-layer substrate needs baking at higher temperature to remove outgassing components, as shown in Figure 4. Substrate pre-bake aimed to get rid of all those components prior to assembly, which could otherwise evaporate during reflow. Although there are many ways to prevent substrate from absorbing moisture after fabrication such as seal in dry air protected bag or sometimes even in vacuum, substrate still contains certain amount of moisture. In

addition, outgassing components always exist in solder mask, which varies according to solder mask type and processing conditions from substrate manufacturers. In some cases, even substrate from same manufacturer gives different results from batch to batch, also as shown in Figure 4. This concern becomes more critical for flip chip assembly process with reflowable underfill as the pre-dispensed underfill as well as the chip on top of it will block outgassing components from escaping out of the package during reflow and at the end turn them to be voids. This phenomenon becomes more severe for multi-layer substrate probably due to thickness factor. In fact, actual pre-bake conditions vary from substrate to substrate and need to be established before assembly.

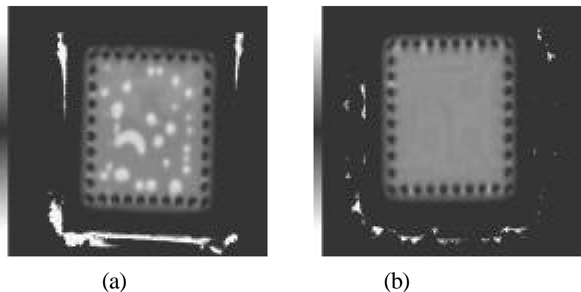


Figure 3. C-SAM images showing effect of substrate (TV1, two layers) pre-bake on void (a) no pre-bake (b) 2h at 125°C

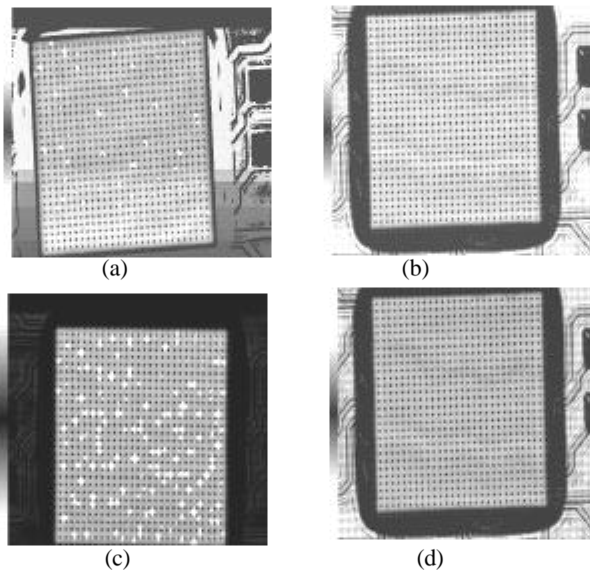


Figure 4. C-SAM images showing effect of substrate (build-up) pre-bake conditions on void (a) 24h at 125°C, batch 1 (b) 3h at 150°C, batch 1 (c) 24h at 125°C, batch 2 (d) 3h at 150°C, batch 2.

Furthermore, delay time after pre-bake but prior to assembly also has to be controlled in order to minimize moisture uptake. Figure 5 shows the voids level of the same test vehicle as in Figure 4 with different delay time. As shown in Figure 5, void increases as extending delay time. In mass production phase, this can be eliminated by means of proper in-line machine integration.

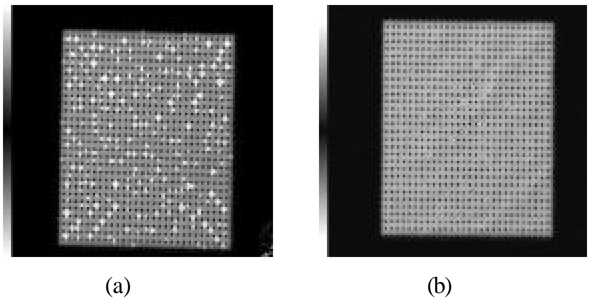


Figure 5. C-SAM images showing effect of delay time on void (a) delay 1h (b) no delay

Underfill dispensing

Figure 6 shows the effects of substrate bond pad design on trapped voids during dispensing.

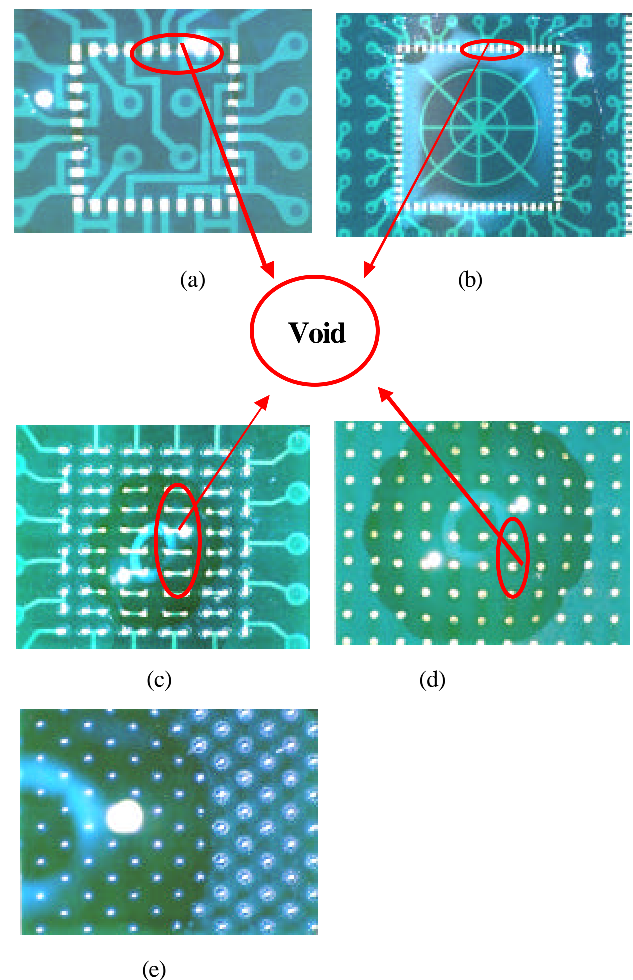


Figure 6. Images showing effects of bond pad design on trapped voids due to dispensing (a) Slot (b) Slot (3 row) (c) Pad define (d) Solder mask define and (e) Pre-solder deposition

As can be seen in Figure 6, more and larger voids have been trapped in slot and pad defined substrates compared to that with solder mask define. Closed inspection unveiled that for slot opening voids are trapped between two adjacent bond pads, while for pad define voids are captured in the clearance area between solder mask and Cu trace. This observation indicated that underfill was not able to flow smoothly over the pad area, where surface was much more rougher than the rest, to exchange the air pocket that has shown stronger resistance of escaping. On the other hand, improvement has been observed in solder mask defined substrate in which only Cu pad is exposed out of solder mask. In the case of pre-soldered substrate, nearly void free can be achieved after underfill dispensing, as shown in Figure 6(e). Figure 7 shows C-SAM images of the 5 test vehicles after assembly. As shown in Figure 7, trapped voids did not escape but instead have merged into larger sizes during reflow and remained inside package.

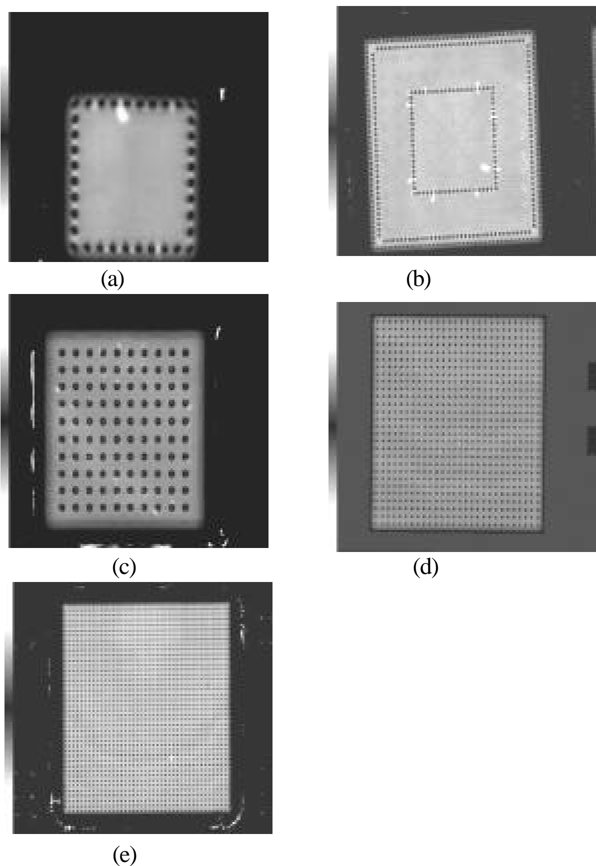


Figure 7. C-SAM images showing effect of various bond pad design on void (a) Slot (b) Slot (3 row) (c) Pad define (d) solder mask define (e) pre-solder.

It is well understood that underfill flowability is dictated by a number of factors, such as underfill surface tension and viscosity, substrate surface tension and roughness as well as temperature etc. Definitely, underfill with higher flowablility with respect to particular substrate surface conditions can be formulated during underfill development stage. However, there is always limitation in increasing flowability via adjusting formulation without deterioration of other material properties. Another way to consider is from assembly process perspectives, in which substrate is being heated during dispensing. Voids are expected to minimize as higher temperature on the substrate surface enables to enhance underfill flow. Figure 8 shows the images of heated substrate surface after underfill dispensing. As compared with Figure 6(a) – 6(c), trapped voids have been tremendously reduced. This fact has also been confirmed by C-SAM images after assembly, as shown in Figure 9. Compared to Figure 7, much improvement has been demonstrated, in addition, it appears that these two substrates with slot design [Figures 9(a) and 9(b)] shows more voids than pad defined design [Figure 9(c)].

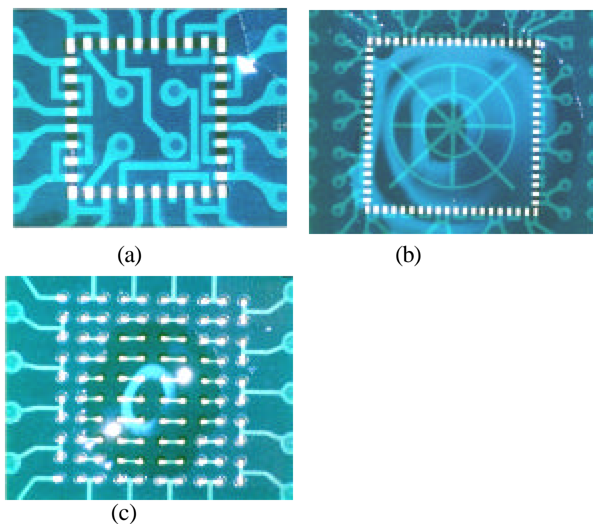


Figure 8. Images showing effects of substrate heating during underfill dispensing on trapped voids by different bond pad design (a) Slot (b) Slot (3 row) (c) Pad define

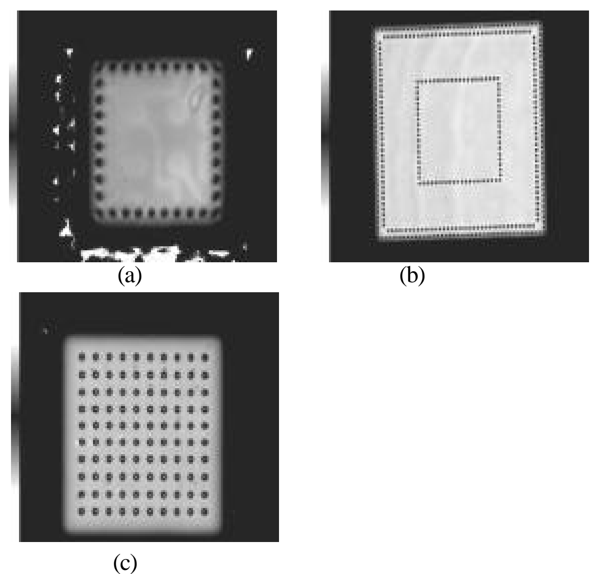
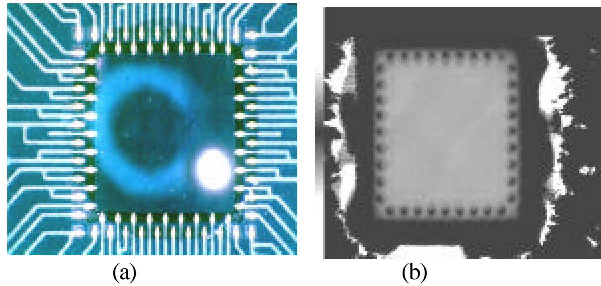


Figure 9. C-SAM images showing effect of substrate heating during underfill dispensing on void (a) Slot (b) Slot (3 row) (c) Pad define

Does the difference result from different pad design or other factors like solder mask thickness? As the two slot designs have the thickest solder mask among all test vehicles, as illustrated in Table 2. To this end, an additional test vehicle with similar slot design was submitted into the same evaluation, where the solder mask thickness was only 28 µm. Figure 10 shows the void level both after underfill dispensing at room temperature and after assembly. As shown in Figure 10, that no trapped voids can be visibly found, which is the reflection of underfill smooth flow over pad area. This fact strongly suggests that thinner solder mask is desired from the standpoint of minimizing trapped voids.

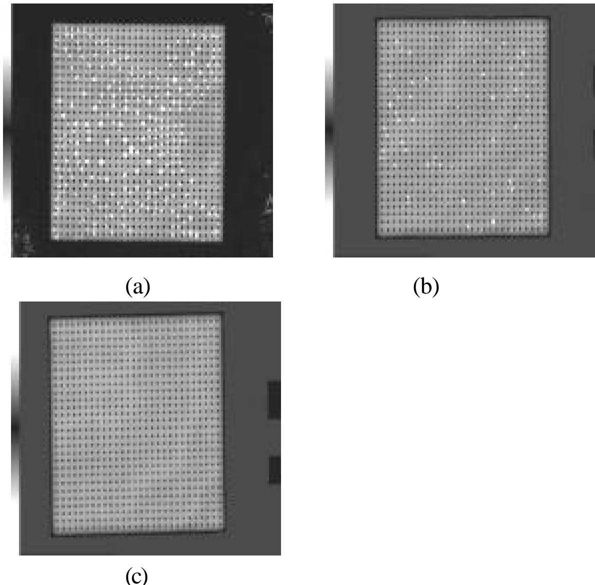


(a) (b)

Figure 10. Effect of thin solder mask (28 µm) on void (a) After dispensing at RT (b) After assembly.

Chip placement

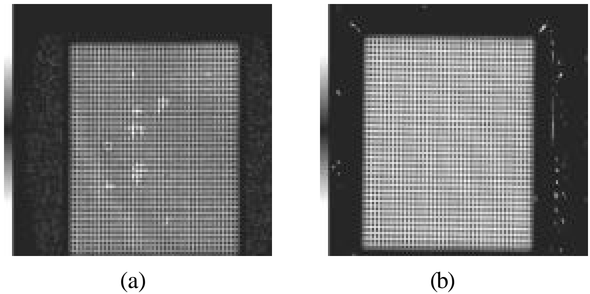
Prior arts have reported that voids could be trapped around bumps during chip placement process [1,2]. In present study, different search speed has been excised to examine the placement influence on void issue. In order to isolate current factor from dispensing, all voids generated during dispensing including those tiny ones have been manually removed prior to chip placement. Also for the sake of justification convenience, underfill was dispensed in cross-pattern over the pad area. Figure 11 shows the dependence of void on search speed. It can be clearly seen that void increases significantly as search speed goes up. More importantly, the voids consistently arranged in the same cross-pattern as that for underfill dispensing and less void have been found in areas where initially dispensed underfill did not cover. This observation disclosed that void was trapped because underfill cannot wet into those bumps that are penetrating into underfill, especially when search speed is high. Once underfill is compressed to flow towards die edges, it tends to wet most of the bumps it passed through. This assumption was supported by observations from Figure 7 (b) and Figure 9 (b) as well, in which most voids were trapped in the inner row. In reality, reducing search speed turns out to affect throughput in mass production phase, as such, is not considered as an efficient method for void minimization. However, same concept as substrate heating can be applied to chip placement. In this case, bond head can be heated to a certain temperature range, for example 80°C~120°C. Thus, when bumps that have started to be heated since die pick-up touch underfill, its viscosity in that localized portion will decrease dramatically and benefit wetting into bumps, in other words minimize voids. Currently, most flip chip bonder vendors enable to incorporate heating element into bonding head. Figure 12 shows the effect of bond head heating during chip placement on void.



(a) (b)

(c)

Figure 11. C-SAM images showing effect of search speed on void (a) 2.4mm/s (b) 1.2mm/s (c) 0.6mm/s



(a) (b)

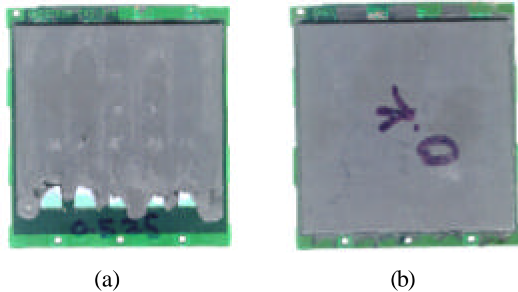
Figure 12. C-SAM images showing effect of bonding head heating on voids (a) without heating (b) heating at 120°C

So far all the discussion encompasses the assembly process and all the voids are attributed to being trapped in assembly. Does underfill outgassing contribute to void formation and to which extent? Thermal Gravity Analysis (TGA) measurement of present formulation has shown about 6.2 % of weight loss when running from room temperature to 230°C at a constant heating rate of 10°C/min. However, there is a big difference between actual heating in reflow oven and testing conditions in TGA, in which temperature ramping rate during reflow is much faster than in TGA. This was translated into shorter heat exposure during reflow. Thus, actual weight loss of reflowable underfill is much lower than that characterized via TGA. In fact, outgassing can only occur when free surfaces for gas escape are granted. This assumption implies that underfill outgassing cannot start given the space underneath the die is void-free after placement. In order to prove that, underfill was applied onto glass slide and then a chip was slowly placed on top. Ensure no any trapped void underneath the die before the whole assembly was placed

on hotplate with glass slide on top for visualization. Hotplate was gradually heated to 230°C, and no outgassing from underfill has been observed. This test has drawn a conclusion that underfill outgassing did not occur if no void has already been trapped in assembly process.

Overmolding

Different from leaded package and BGA, some constrain needs to be taken into consideration when overmolding eutectic solder bumped flip chip package that has been underfilled. Improper molding condition could damage underfill fillet as shown in Figure 13, in some cases even pull out the chips from substrate.

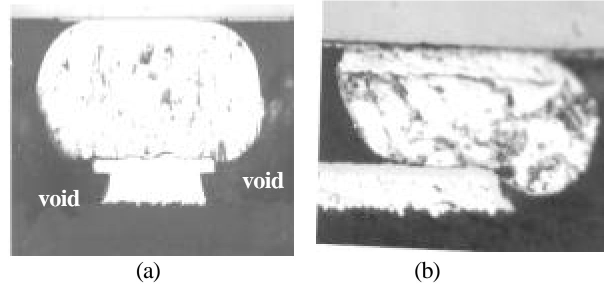


(a) (b)

Figure 13. Flip chip package with overmolding by (a) improper condition (b) optimized condition

Reliability

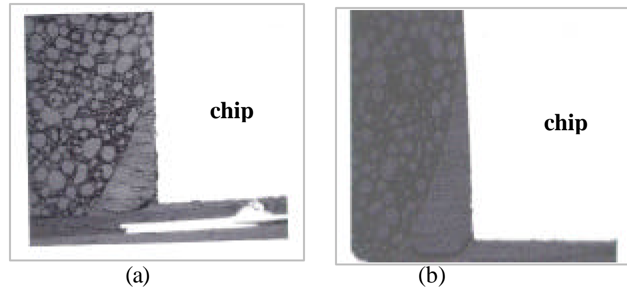
The reliability results of TV1~TV4 were summarized in Table 3. For TV1 and TV2 (overmold), all units have passed 1000 TCT while certain percentage of failure has been found for other four test vehicles. It appears that overmold does not increase the number of cycles to failure under thermo-mechanical stress, but may create defect that will accelerate failure rate if overmold process was not optimized like TV1 overmold case. Failure analysis has revealed that typical failure mode is solder crack for both TV1 (overmold) and TV3 while poor solder wetting causes failure of TV2 and TV4, as shown in Figure 14. It became obvious that cracked bumps have been isolated from underfill by large voids, which corresponds very well with earlier discussion that there were more voids in TV1 and TV3 compared to the rest. This fact shows assembly process limitation in void removal. As a result, fabrication of substrate with thinner solder mask must be undertaken to more effectively reduce void and deliver better package reliability.



(a) (b)

Figure 14. Cross-section view of (a) bump crack (TV3) (b) dry joint (TV4)

Flip chip with overmolding is a new package structure, in which the interface between mold compound and underfill is a big concern. Figure 15 shows the cross-section images of both TV1 and TV2 with overmolding after 1000 cycles TCT. No delamination between mold compound and underfill has been observed. Nevertheless underfill fillet crack at die corner does exist, which most probably arises from high stress generated during TCT. Although underfill crack does not cause electrical failure immediately like TV2 overmold case in this study, it could propagate into mold compound and easily induce substrate crack, delamination at underfill/substrate, underfill/mold compound, mold compound/substrate and solder fatigue as well.



(a) (b)

Figure 15. Cross section view of overmolded flip chip via reflowable underfill process (a) TV1 (b) TV2.

Table 3 Summary of reliability results for flip chip assembly with reflowable underfill

Test Vehicle	Failure Rate of Thermal Cycle Test (TCT, -55°C ~ 125°C)					
	After pre-con	250	550	750	1000	Total
TV1	0/32	0/32	0/32	0/32	0/32	0/32
TV1 overmold	0/32	0/32	1/32	1/31	7/30	9/32
TV2	0/32	2/32	0/30	0/30	0/30	2/32
TV2 overmold	0/32	0/32	0/32	0/32	0/32	0/32
TV3	0/32	1/32	1/31	0/30	1/30	3/32
TV4	2/32	1/30	0/29	1/29	1/28	5/32

Conclusion

In this paper the influence of assembly process on void has been extensively studied. Voids were found to be trapped in bond pad area during underfill dispensing and chip placement and could not escape during reflow. Bond pad design also has great impact on void level, where pre-soldered substrate trapped least void. Underfill flowability was the key to minimize void. As such, substrate heating during underfill dispensing as well as bond head heating during chip

placement have been proposed, and proven to be effective for removing voids. Thinner solder mask is preferred from the standpoint of minimizing void also. Furthermore, reliability and failure analysis were also studied. It was found that bumps that have been isolated from underfill because of voids were prone to crack.

References

1. N.W. Pascarella and D.F. Baldwin, "Compression Flow Modeling of Underfill Encapsulants for Low Cost Flip Chip Assembly," 4th International Symposium on Advanced Packaging Materials, Braselton, GA, March 1998

2. R.Thorpe, D.F. Baldwin and L.P. McGovern, "High Throughput Flip Chip Processing and Reliability Analysis Using No-Flow Underfills," IEEE 49th ECTC Proceedings, San Diego, CA, 1999.