Studies on A Novel Flip-Chip Interconnect Structure – Pillar Bump

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Abstract

Pillar bump is a novel interconnect structure, including non-reflowable base and a reflowable cap like a pillar shape. In this study, pillar bump with copper base and Sn63/Pb37 eutectic solder cap is processed via electrolytic plating. Based on whether flat eutectic cap is reflowed prior to assembly, pillar bump is further split into two categories, namely pre-reflowed and non-reflowed, respectively. Assembly feasibility assessment as well as bump integrity evaluation are carried out. Bump shear test is conducted for both before and after reliability and failure mode is characterized via SEM and EDX. Furthermore, a 10 mm x 10 mm test chip having 180 Cu/eutectic solder pillar bumps with 0.2 mm pitch is assembled onto BT substrate via no clean flux and subsequently underfilled. The results show that pillar shape is still maintained after assembly that can meet fine pitch requirement. No shear strength deterioration after moisture sensitivity preconditioning and 1000 thermal cycle test (TCT, -40°C ~ 125°C) has been observed. EDX spectra indicate fracture has occurred in the interfacial region between Al and silicon, not arising from bumping process. Furthermore, bump integrity is intact after package level reliability test under the same conditions as above. Stress simulation results lead to conclusion that maximum shear stress occurs in copper pillar portion with average range of 40 ~ 50 MPa that is much below the shear strength of copper.

Introduction

Solder bump is the key component for flip-chip interconnection. Starting with C4 process from IBM, several alternative bumping methods have been successfully developed during the past decades. On the other hand, most of current bumping technologies is facing challenges in fine pitch application that is being driven by high density and product miniaturization requirement. Pillar bump is a novel interconnect structure, including non-reflowable base and reflowable cap like a pillar shape, as shown in Figure 1. Pillar bump has a high aspect ratio that allows fine pitch bumping. In addition, as the base material is non-reflowable, standoff can be maintained, which will deliver high reliability package and facilitate underfill flow as well. More importantly, pillar bump composition is flexible such as copper base with eutectic solder cap, high lead solder base with eutectic solder cap as well as copper base with lead-free solder cap, just name a few. Functionally, larger gap between lead and chip active surface, which resulted from pillar bump with non-lead base, enables to reduce α- emission effect that can cause soft error in certain devices, especially memory chips.

In this study, pillar bump with copper base and Sn63/Pb37 eutectic solder cap is processed via electrolytic plating while focus is on chip assembly assessment as well as bump integrity evaluation via reliability test. In addition, Finite Element Analysis (FEA) is used to simulate stress distribution in pillar portion when cyclical forces are being applied.

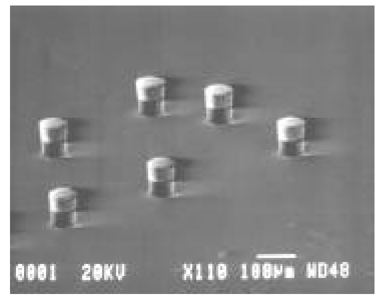


Figure 1 Images of Pillar Bump

Experimental

1. Bumping

The chip used in this study is a 10 x 10 mm peripheral bumped daisy chain test die. Cu/eutectic solder (50μm/50μm) pillar bump was electrolytically plated with 1000Å Ti as Under Bump Metallurgy (UBM).

2. Die Shear Test

According to the shape of eutectic solder cap, shear test was conducted for both non-reflowed and pre-reflowed bumps via Dage 2400. Shear blade height was set at 30 μm and 70 μm, respectively, in order to obtain shear strength values at different interfaces, as schematically sketched in Figure 2.

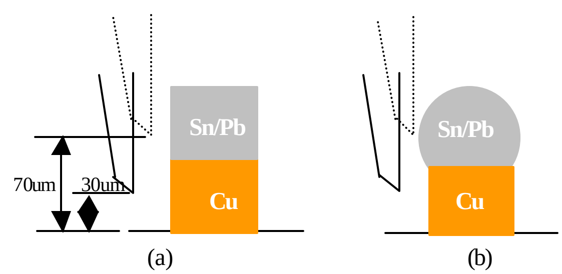


Figure 2. Schematic diagram for pillar bump shear test (a) Non-reflowed (b) Pre-reflowed

3. Chip Assembly

Test vehicle details are listed in Table 1. 32 units each for both types of bump were assembled via conventional underfill process. Chip placement was carried out via Micron II flip-chip bonder. Heller 1800W was used for reflow. Standard SMT reflow profile was adopted with peak temperature at 220°C. Underfill dispensing was manually conducted on hot plate.

Table 1. Test vehicle details

Chip	Format	Peripheral
	Die passivation	SiN
	Die size	10 x10 mm
	No. Of bumps	180
	Pitch	200 µm
	Bump height	60 µm/60 µm
	Bump material	Cu/Sn63/Pb37
Substrate	Type	BT laminate
	No. Of die/ Sub.	36
	Sub. Thickness	0.32mm
	Surface finish	Ni/Au

4. Reliability

Moisture sensitivity preconditioning (30^oC/70%RH for 120h) together with three times oven reflow with peak temperature of 240^oC was conducted prior to thermal cycling test (-40^oC ~ 125^oC). Dwell time at each end was 15 min. C-SAM was used to examine the voids as well as delamination, and conducted for all the units both before and after reliability.

Results and Discussion

1. Assembly Feasibility

Pillar bump structure was studied for both non-reflowed and pre-reflowed bumps. Figure 3 shows cross section view of both types and the corresponding dimension was listed in Table 2. As clearly shown in Figure 3(b) and 3(d), eutectic solder cap that was originally in column shape has formed into a sphere after one time reflow prior to assembly. In addition, the eutectic solder cap just reformed its shape rather than wrapping upward along Cu base, which is desired in order to keep the merit of pillar bump. Table 2 indicated that actual bump height was consistent with specification of 60µm/60µm, which shows good plating process control. Various dimensions between both types fall into the same range except that pre-reflowed bumps demonstrated a higher overall bump height that could facilitate underfilling process.

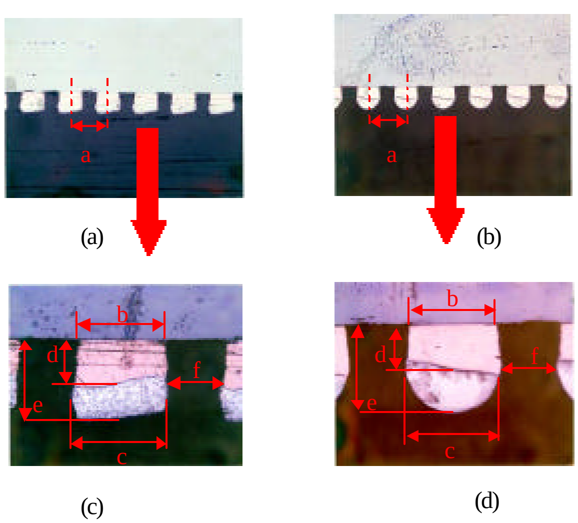


Figure 3. Cross section view of pillar bump structure for (a) and (c) Non-reflowed (b) and (d) Pre-reflowed

Table 2. Pillar bump dimensions

		Non-reflowed bump (µm)	Pre-reflowed bump (µm)
a	Bump Pitch	200	200
b	Pillar dia. (Cu)	115 to 120	115 to 120
c	Pillar dia. (Solder)	128	123
d	Pillar height (Cu)	58	58
e	Overall height	105	115
f	Bump gap	75	75

Figure 4 shows the cross section photos of both pre-reflowed and non-reflowed pillar bumps after flip chip assembly. In the former case, it can be observed that pillar shape is still maintained after assembly to meet fine pitch requirement. More importantly, the resultant large gap between solder and chip active surface can reduce α-emission impact on certain functional chips. But for the latter one, solder cap has wrapped upward and covered Cu base, which to a certain extent lost the merits of pillar bump. Furthermore, spherical solder cap is preferred from assembly process standpoint, for example, it is easier to form contact with bond pad in substrate especially when solder mask opening is smaller.

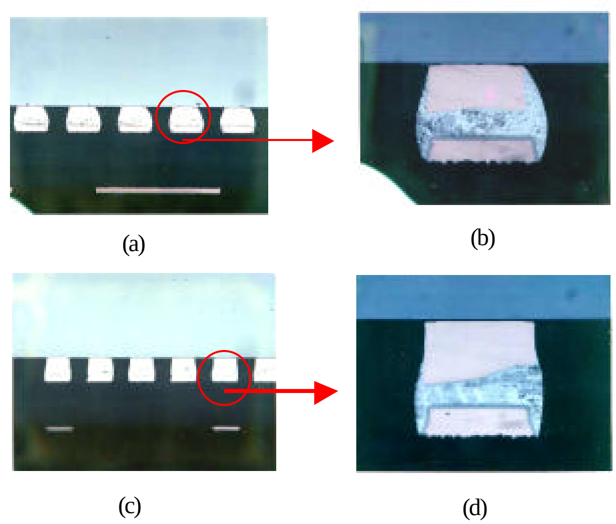


Figure 4. Cross section for pillar bumps after assembly. (a) and (b) No-reflowed (c) and (d) Pre-reflowed

2. Bump Integrity

Five chips each for both pre-reflowed and non-reflowed pillar bumps were used for bump shear test. The results were tabulated in Table 3. Each value shown in Table 3 is the average of 100 readings. As shown clearly in Table 3, no bump shear strength deterioration has been observed after thermal cycling for 1000 cycles. In general, interface between Cu and solder expresses lower adhesion strength in comparison with that between Cu and chip surface. Figure 5 and Figure 6 shows SEM images and EDX spectra of fractured interfacial region after bump shear (height=30 µm) for both before and after stress test. It was found that only Al and Si signals were detected for both cases, which implied that fracture has occurred in the interfacial region between Al and Si. This observation suggests that adhesion strength between Ti UBM and Cu is superior and able to keep bump integrity throughout the stress test.

Table 3. Shear strength for pillar bump before and after reliability

Reliability	Non-reflowed		Pre-reflowed	
	Shear Strength (g)		Shear Strength (g)	
	30 µm (Height)	70 µm (Height)	30 µm (Height)	70 µm (Height)
Pristine	137	35	123	45
After Pre-conditioning	129	55	129	52
125 cycles	133	46	126	45
520 cycles	136	46	130	45
1000 cycles	131	45	129	43

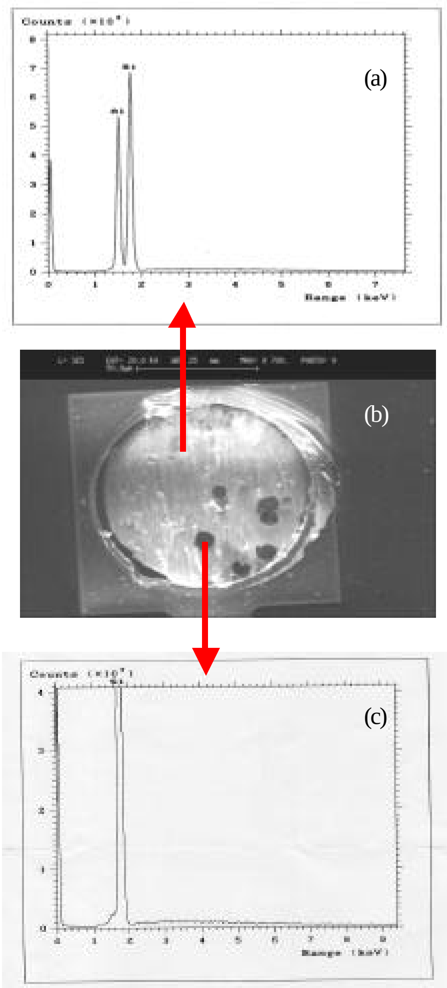


Figure 5. Images of fractured interfacial region before stress test. (b) SEM image (a) EDX spectra of bright portion (c) EDX spectra of dark portion.

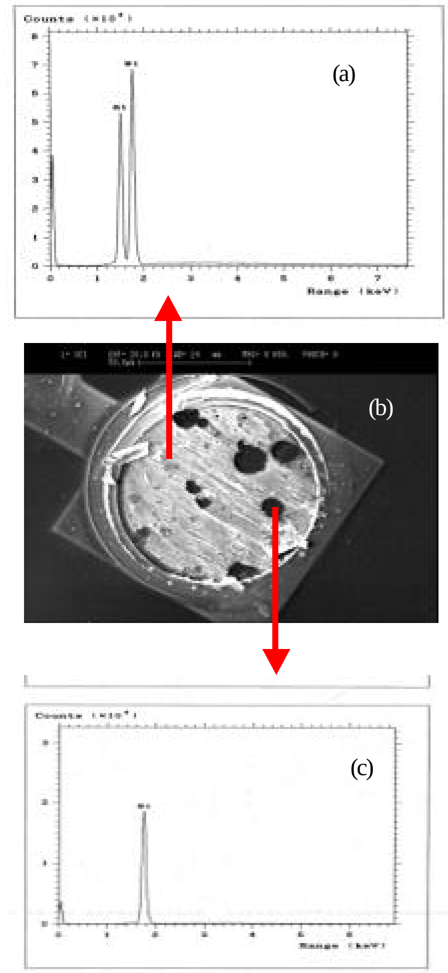


Figure 6. Images of fractured interfacial region after stress test. (b) SEM image (a) EDX spectra of bright portion (c) EDX spectra of dark portion.

With regard to package level reliability, about 30% units have electrically failed after moisture sensitivity preconditioning due to delamination between underfill and chip passivation, as shown in Figure 7. As the failure did not result from bump, the survived units still proceed with thermal cycle test (TCT) and no further failure was detected up to 1000 cycles. Figure 8 shows the cross section images of both pre-reflowed and non-reflowed pillar bumps after TCT 1000 cycles. As shown in Figure 8, bump still maintain pillar shape, in particular no bump crack has been observed. On the other hand, compared to Figure 4 solder has wrapped upward along the Cu base even for pre-reflowed pillar bump. This probably has occurred during three times reflow after moisture sensitivity preconditioning, in which solder repeatedly melt and wet the Cu portion. Although fine pitch requirement still can be met in the present case, effect of α-emission reduction will be weakened. Thus, pre-treatment of Cu base prior to reflow is needed to prevent solder from wrapping up during subsequent assembly process. Meanwhile, the amount of flux and method to apply it play an important role also.

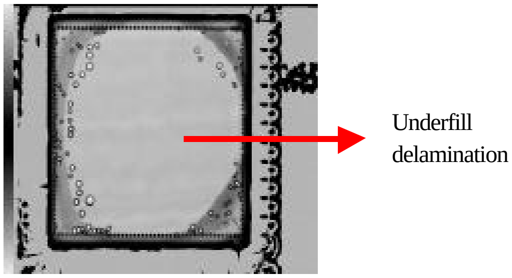


Figure 7. C-SAM images after moisture sensitivity conditioning

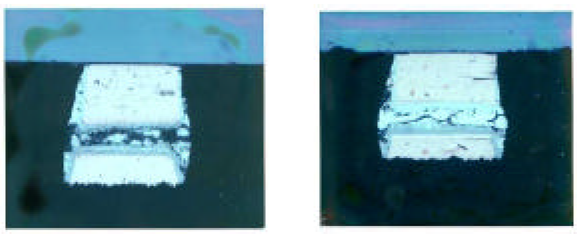


Figure 8. Cross-section images of pillar bump after TCT 1000 cycles (a) pre- reflow (b) non-reflow

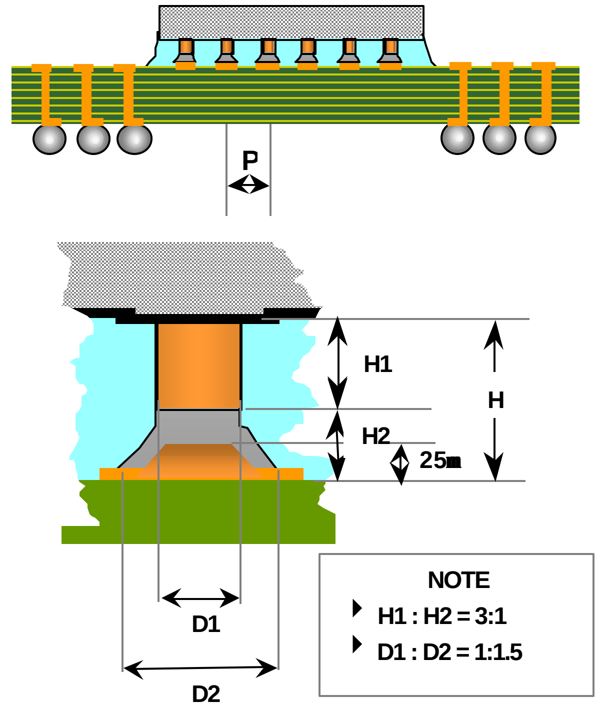


Figure 9. Schematic drawing of bump geometry considered.

3 Pillar Bump Stress Analysis

To understand the stress distribution during stress test of pillar bumped flip chip package, and thus optimize bump design for improved reliability, pillar bump stress analysis was generically performed. The assumptions are listed as:

- Die is fully populated array, which is different from the test die used in the present study
- Array is symmetrical around its center
- Stresses arise due to thermo-mechanical mismatch in CTE that results from temperature loading.
- Model assumes constant values for young's modulus and CTE
- No void or delamination is present in materials
-

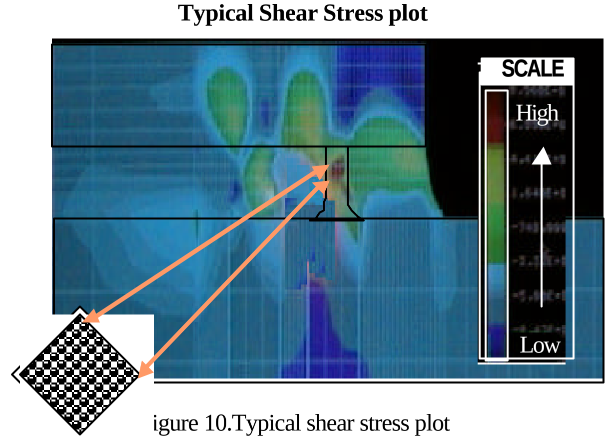
The bump geometry considered are schematically shown in Figure 9 and tabulated in table 4.

Table 4. Bump geometry considered

Die Size (mm)	Bump Pitch P (µm)	Bump Height H (µm)	Bump Diameter D (µm)
15 x 15	100	100	60
	120	100	60
20 x 20	100	100	60
	120	100	60
	160	100	100
	225	100	100
	100	125	100
	120	125	100
	160	125	100

Typical shear stress plot and shear stress distribution in various cases listed in Table 4 were shown in Figures 10 – 13, respectively.

Typical Shear Stress plot



igure 10.Typical shear stress plot

It was observed that maximum shear stress occurs at bumps nearest to die corner. It is in the range of 40 –55 MPa. This stress is much lower than the shear stress of Cu, which is more than 100 MPa. This fact means that pillar bump with above dimension can withstand current stress level without failure. It was also noticed that as the pitch increases, die stresses and shear stresses come down. This is because of additional cushioning effect of the underfill, as such, recommended pitch should be around 1.75 times bump diameter. Similarly, the shear stresses decrease with decreasing bump diameter but increasing bump height. The latter observation resulted from fact that CTE mismatch between substrate and die gets spread over increased gap.

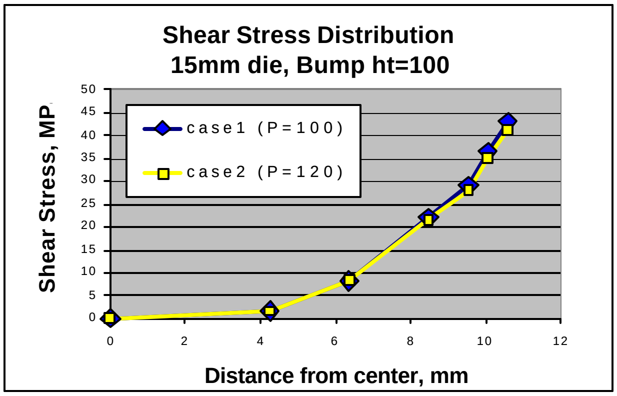


Figure 11. Effect of bump pitch on shear stress

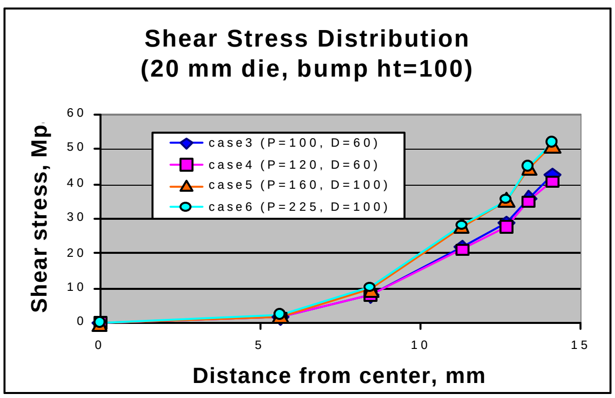


Figure 12. Effect of bump pitch and diameter on shear stress for 20 mm die with 100 µm bump height

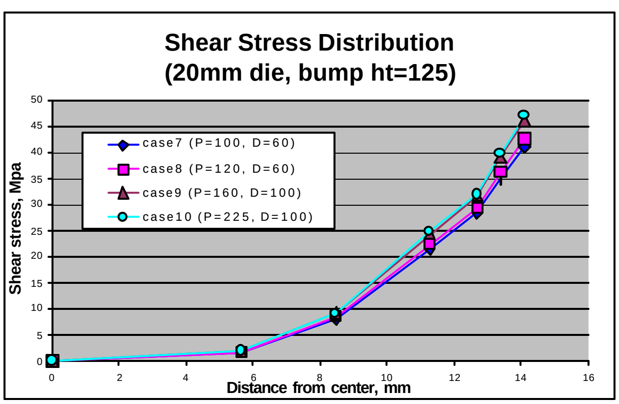


Figure 13. Effect of bump pitch and diameter on shear stress for 20 mm die with 125 µm bump height

Stress simulation for Sn-Pb eutectic solder bump was also carried out. The maximum shear stress in the corner reduces from 52 to 45 MPa in the solder column when the copper pillar is replaced completely by Pb-Sn eutectic. Although the shear stress is reduced, the new maximum shear stress level is still above the shear strength of Pb-Sn eutectic that is about 24 MPa, and so the solder joint will be more prone to fatigue failure compared to the pillar bump with copper. It can be also observed from Figure 10 that stress generated in eutectic solder portion as well as Cu-eutectic solder interface are negligible under current assumption (H1:H2=3:1). This observation suggests that larger height ratio of Cu to solder is preferred from standpoint of reducing the probability that failure occurs in solder portion. Although there is a deviation between the assumption in stress simulation and package conditions used in present reliability study, the current simulation still serves as a guideline to design pillar bump structure.

Conclusion

Chip with pillar bump consisting of Cu base and eutectic solder cap has been successfully assembled onto BT substrate. Both non-reflowed and pre-reflowed bumps have been evaluated. No bump related failure has been found after TCT 1000 cycles. Stress simulation suggests that maximum shear stress fall into the range of 40-55MPa and occurs at upper portion of Cu base whose shear strength is more than 100 MPa. Pillar bump with Cu base and eutectic solder cap has higher resistance to fatigue failure in comparison with pure eutectic solder bump.