

RELIABILITY STUDIES OF FLIP CHIP PACKAGE WITH REFLOWABLE UNDERFILL

Tie Wang, T.H. Chew, Y.X. Chew and Louis Foo
Questech Solutions Pte Ltd
Singapore 739256

ABSTRACT

Reflowable underfill is originated to simplify the Flip-Chip assembly process. In this study, JEDEC level 3 moisture sensitivity preconditioning followed by thermal cycling (TCB, -55°C ~ 125°C) was conducted. Two reflowable underfill mainly differentiated by curing kinetics and adhesion strength, namely Underfill A and Underfill C, were evaluated. Failure analysis was carried out via C-SAM and cross section. Unit failure that was electrically identified in present study was defined as occurrence of bridging and/or open circuit. The results showed that for packages assembled with Underfill A that has superior adhesion with silicon nitride passivation, all units can pass preconditioning but bridging commenced to appear at 750 cycles. Open circuitry was encountered between 1750 and 2000 cycles. While for Underfill C with fast cure characteristics and relatively weaker adhesion compared to Underfill A, bridging and open circuitry started to surface at 500 and 1250 cycles, respectively. Failure analysis indicated that bridging mainly resulted from solder bump extrusion through micro voids trapped between adjacent bumps during assembly process; meanwhile the gap between neighboring bumps is too close to prevent convergence of two extruded bumps. Open circuitry is originated by several factors such as insufficient wetting, underfill delamination, die crack, underfill crack etc.

On the whole, no underfill delamination and die crack have been observed before 1000 cycles in present study. Most importantly, no solder crack that is the direct reflection of CTE mismatch has been observed throughout the whole reliability test. This fact suggests that assemblies with relatively-higher-CTE reflowable underfill still can meet general reliability standard.

Key words: Flip-chip, reflowable underfill, adhesion.

INTRODUCTION

Reflowable underfill is the integration of epoxy and flux. It possesses self-fluxing capability to make solder bump reflow and underfilling process occur simultaneously [1-3]. As such, Flip-Chip assembly with reflowable underfill has advantages over conventional process using capillary-flow underfill in terms of process flow and capital investment, as schematically shown in Figure 1. On the other hand, due to solder bump interconnection yield concern, reflowable underfill is inherently an unfilled system i.e. no silica filler in formulation with relatively

higher coefficient of thermal expansion (CTE, 70~90 ppm/ $^{\circ}\text{C}$). Theoretically, underfill with higher CTE cannot solve CTE mismatch issue efficiently which could cause earlier loss of solder joint integrity due to thermo-mechanical failure generated during thermal cycling test (TCT). Therefore, reliability has to be proven before Flip-Chip assembly with reflowable underfill becomes a real solution. Nevertheless, fewer reliability results associated with failure analysis have been reported so far. The goal of this study is to understand the reliability performance of Flip-Chip package assembled with reflowable underfill as well as various failure modes.

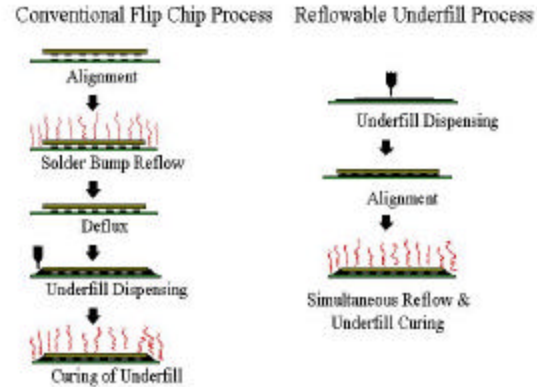


Figure 1. Schematic diagram of Flip Chip assembly both with reflowable and conventional underfill

EXPERIMENTAL

Material characterization

Both Underfill A and C were formulated in house. The epoxy resin, hardener, catalyst and wetting precursor were purchased from commercial sources and used as received.

DSC studies were performed via a modulated DSC (TA Instruments, Model 2920). Approximately 10mg of samples were used for each run and ramping rate was kept at $10^{\circ}\text{C}/\text{min}$. Die shear test was used to measure adhesion strength of underfill with chip passivation. Dummy chips with certain passivation layer, such as silicon nitride and polyimide in the present study, were bumped with peripheral arranged eutectic solder bump that is served as spacers to precisely maintain stand-off during shear test. Firstly, one droplet of underfill was put onto the center of chip; then the chip was mounted on stainless steel plate and the whole assembly passed through reflow oven and was subsequently postcured according to respective

underfill material specification. The cross view of set-up for die shear test was illustrated in Figure 2. Similarly, the adhesion strength between underfill and solder mask was measured as well, in which substrate coated with solder mask was mounted onto stainless steel plate. Adhesion strengths were tested both before and after moisture sensitivity preconditioning (85°C/85%RH, 168h) in order to assess the heat/humidity effect on underfill adhesion. 30 samples were chosen for each test.

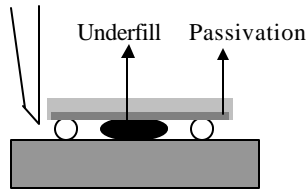


Figure 2. Cross view of die shear test set-up

Flip chip assembly

The test vehicle used in this study consists of a 10 x 10 mm peripheral bumped, daisy chain test die mounted on BT substrate. The details are listed in Table 1. Underfill dispensing and chip placement were carried out via Micron II flip-chip bonder. Heller 1800W was used for reflow. Standard SMT reflow profile was adopted with peak temperature at 220°C.

Table 1. Test vehicle details

Chip	Format	Peripheral
	Die passivation	SiN
	Die size	10 x10 mm
	No. of bumps	180
	Pitch	200 μm
	Bump height	95μm
	Bump diameter	135μm
	Bump material	63Sn/37Pb
Substrate	Type	BT laminate
	No. of die/ Sub.	36
	Sub. Thickness	0.32mm
	Surface finish	Ni/Au

Reliability and failure analysis

JEDEC level 3 moisture sensitivity preconditioning together with three time oven reflow with peak temperature of 230°C were conducted prior to thermal cycling test (TCB, -55°C ~ 125°C). Dwell time at each end was 15 min. In addition, HAST (130°C/85%RH, 75h) has been performed for package assembled with Underfill A. GSAM was used to examine the voids as well as delamination, which was conducted for all the units both before and after reliability. Other failure modes like bridging and underfill fillet crack were mainly observed via cross section.

RESULTS AND DISCUSSION

Underfill characterization

Two reflowable underfill materials with different curing profile were formulated and evaluated in this study. Underfill C has faster curing characteristics than Underfill A, which can be translated into shorter postcure time requirement, or even no need postcure under specific reflow profile. The corresponding DSC curves can be found in our previous publication [2]. Table 2 shows the summary of adhesion strengths between underfill and various surfaces both before and after moisture sensitivity preconditioning.

Table 2. Summary of underfill adhesion strengths with various surfaces.

	Underfill A		Underfill C	
	Before (psi)	After (psi)	Before (psi)	After (psi)
SiN	11,300	8,100	8,200	5,500
PI	12,100	6,700	7,700	4,500
Solder Mask	6,700	5,700	6,000	3,200

It can be readily observed that Underfill A has stronger adhesion strengths with respect to the three surfaces in comparison with Underfill C. The superior adhesion of Underfill A probably resulted from the particular epoxy system being used for this formulation. For Underfill A, adhesion with respect to passivation is almost double that to solder mask while Underfill C does not show significant adhesion difference to all the three surfaces. In general, higher strength to passivation layer has been pronounced for both reflowable underfill materials. Their absolute values are at least not inferior to, but to a certain extent even better than those of conventional capillary flow underfill. After preconditioning, adhesion strengths to SiN and PI have dropped 30% and 40%, respectively, for both underfill. On the other hand, for Underfill A 85% of adhesion to solder mask can still be retained contrast to almost 50% decrease for Underfill C.

Thermal cycle and HAST

The thermal cycle results for both underfill were reflected in Figure 3, which included two batch assemblies with Underfill A and one batch with Underfill C. The details of failed units were summarized in Table 3 in terms of either bridging or open circuit. It can be seen that all units can pass JEDEC level 3 moisture sensitivity preconditioning. For Underfill A, bridging and open circuit started to appear at 750 and 1750 cycles, respectively. In the case of Underfill C, the same failure was encountered as earlier as 500 and 1250 cycles, respectively. In addition, no delamination between Underfill A and chip passivation SiN/solder mask has been found. On the other hand, delamination of Underfill C with both passivation and solder mask commenced to occur after 1250 cycles.

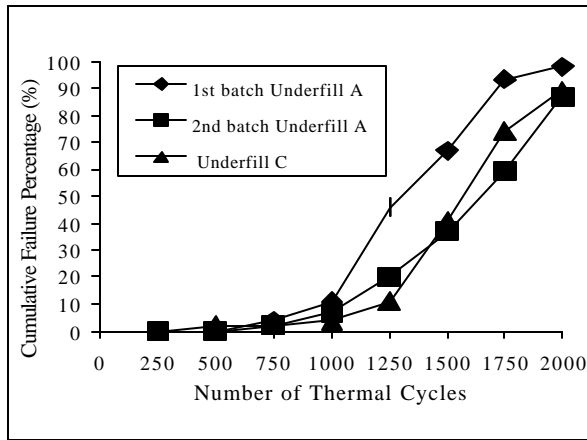


Figure 3. Summary of thermal cycle test results

Table 3 Summary of failed units after thermal cycling

Cycles	Underfill A 1 st batch	Underfill A 2 nd batch	Underfill C
after precondition			
250			
500			1B
750	2B	1B	
1000	2B	2B	1B
1250	16B	6B	1B+2OL
1500	10B	12B	14B
1750	10B+2OL	10B	13B + 2B&OL
2000	2B	8B + 1B&OL	6B + 1B&OL
Total	42B+ 2OL	39B + 1B&OL	36B+2OL+3 B&OL

All samples assembled with Underfill A has passed HAST, and no electrical failure and underfill delamination have been observed, as shown in Figure 4.

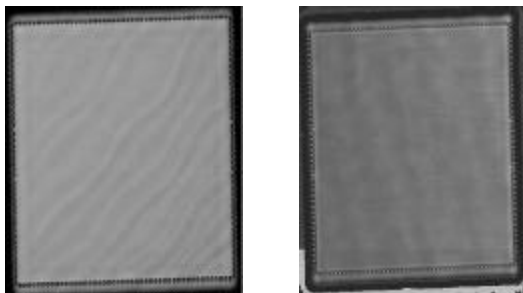


Figure 4. CSAM images of a typical unit (a) before and (b) after HAST

Solder bridging

As shown in Table 3, bridging was the most predominant failure mode that has been observed for this test vehicle

assembled with both underfill. Figure 5 clearly depicts the cross section images of two bridged bumps. As shown in Figure 5, the bridging is caused by solder extrusion that is the growth of solder bump into a void inside underfill. Once solder extrusion from adjacent bumps converges, it causes bridging and can even result in open circuit over time.

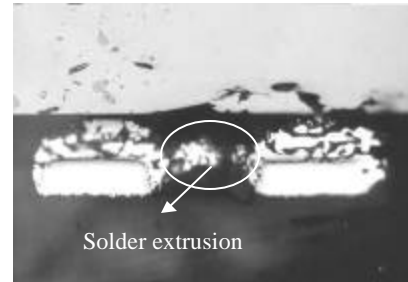


Figure 5. Cross-section images of solder extrusion

Solder extrusion results from CTE mismatch among various components in flip chip package during TCT, which cannot be avoided given existence of voids in underfill. In some cases, voids can hardly be detected via C-SAM due to small sizes, but enable to induce solder extrusion. Furthermore, the gap between neighboring bumps after reflow is only $40\mu\text{m}$, which is too narrow to prevent bridging in the present test vehicle, as shown in Figure 6. The narrow gap arises from bumping as well as corresponding substrate design defect that has produced over-sized bumps in current fine pitch package. Prior art also reported that the variables that modulate solder bump extrusion were voids count, bump pitch, layout, underfill properties and temperature cycle condition [4]. As such, package design such as bump size and substrate bond pad layout according to pitch requirement, in particular for fine pitch packages, plays a significant role in order to reduce bridging probability. Meanwhile, it is equally critical to minimize void count in underfill by all the means like underfill formulation and assembly process optimization.

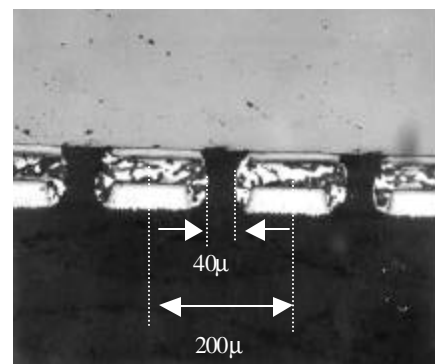


Figure 6. Cross-section view of assembled package

Insufficient wetting and die crack

As indicated in Table 3, two units from Underfill A 1st batch has shown open circuit at 1750 cycles. Figure 7 shows the CSAM images of the two failed units after TCT. As can be seen from Figure 7, one unit did not show distinct failure while die crack was clearly detected for another unit.

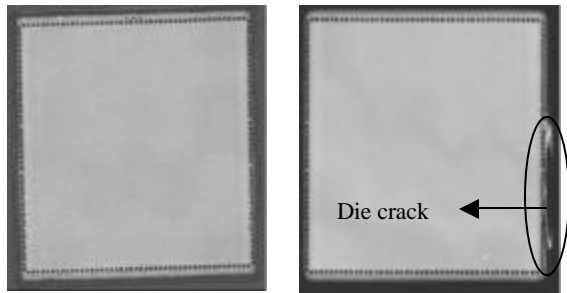


Figure 7. CSAM images of two units from Underfill A 1st batch showing open circuit after TCT 1750 cycles

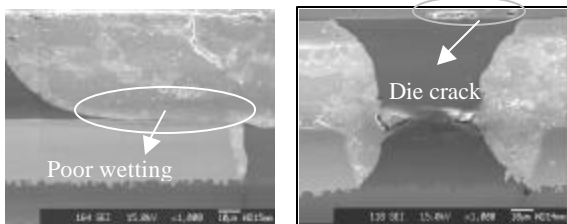


Figure 8. Cross section of two units from Underfill A 1st batch showing open circuit after TCT 1750 cycles

Cross section was carried out to further analyze the failure mode. As shown in Figure 8, insufficient wetting from one bump has been observed for the unit whose C-SAM image did not show obvious failure mode. This poor wetting probably resulted from small bump size or substrate bond pad contamination but not due to underfill material. Die crack can be observed for another unit in agreement with CSAM reflection. In addition, underfill crack beneath die crack region has also been observed. This observation implied that die crack maybe the result of underfill crack.

Underfill delamination

It is well understood that underfill delamination is dictated by adhesion strengths of underfill with both chip passivation and solder mask, especially after moisture sensitivity precondition. Superior adhesion of Underfill A with various surfaces has been demonstrated via shear test as shown in Table 2, which was translated into no observed delamination. As such, failure analysis on delamination in present study is exclusively for units assembled with Underfill C. Figure 9 shows the C-SAM images of one unit that has electrically failed after TCT. Delamination can be seen on the upper left hand corner portion, which is the reflection of DNP effect during stress test. In order to further study delaminated interface,

cross-section in delamination area was also conducted. As illustrated in Figure 10, delamination between underfill and chip passivation SiN has been identified.

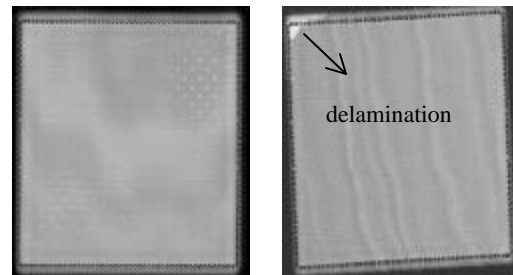


Figure 9. CSAM images of unit assembled with Underfill C (a) before and (b) after TCT

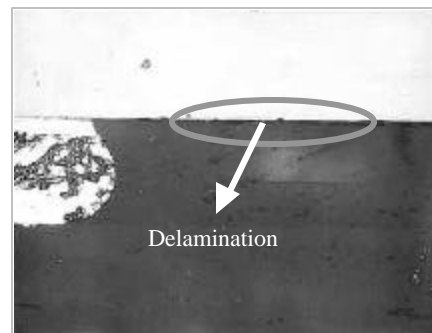


Figure 10. Cross-section view to show delamination at underfill/passivation interface.

Apart from delamination at underfill/passivation interface, delamination was found to occur at underfill/solder mask interface as well in some units. The C-SAM images and cross-section view were shown in Figure 11 and Figure 12, respectively. Again, the delamination occurred at the corner where the highest stress was generated. In worse case, delamination at both interfaces can be observed in same unit, as shown in Figure 13.

Although delamination at both interfaces has been detected in flip chip packages assembled with reflowable underfill, this phenomenon occurs only after 1000 cycles during TCT, which can meet the requirement of most consumer products.

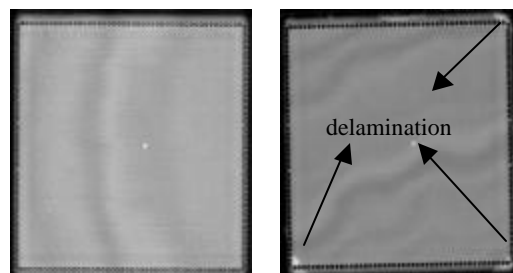


Figure 11. C-SAM images of unit assembled with Underfill C (a) before and (b) after TCT

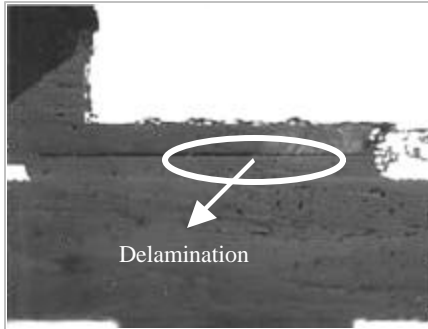


Figure 12. Cross-section view to show delamination at underfill/solder mask interface.

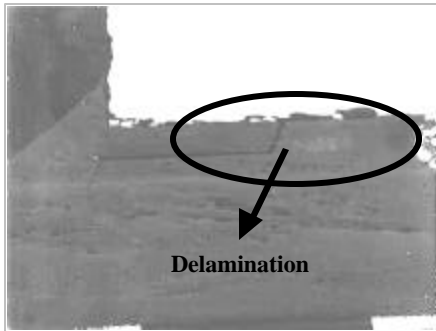


Figure 13. Cross-section view to show delamination at both underfill/passivation and underfill/solder mask interfaces.

Underfill crack

Underfill crack, generally exemplified as fillet crack, has been found for both underfill material but only after 1000 cycle TCT. Figure 14 and 15 show fillet crack from one unit that was assembled with Underfill A and has undergone 1250 and 2000 cycles, respectively. It is obvious that crack propagates during stress test and has reached to the top of the chip after 2000 cycles. In addition, it was noticed that cracks had been initiated from substrate via hole. Figure 16 shows cross section view of the corresponding substrate in which underfill fillet crack has occurred. As shown in Figure 16, there is a distinct crack mark inside via hole plugging material. This observation suggested that plugging material cracked first due to cyclic stress exerted and further transferred the stress to underfill and cause it to crack. The deduction implied that inappropriate plugging material selection could affect underfill integrity, and as a result, deteriorate flip chip reliability. In general, material with certain ductility is needed as via hole plugging material in flip chip application.

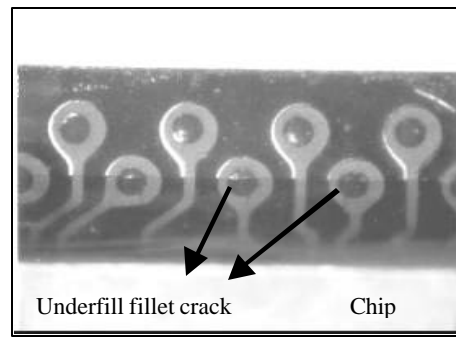


Figure 14. Underfill fillet crack observed at 1250 cycles

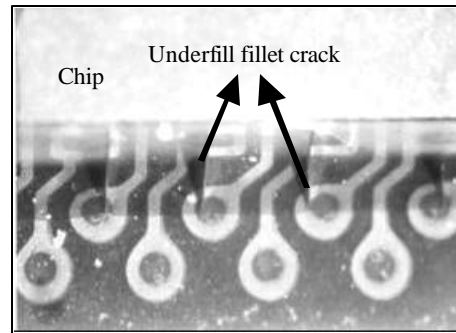


Figure 15. Underfill fillet crack observed at 2000 cycles

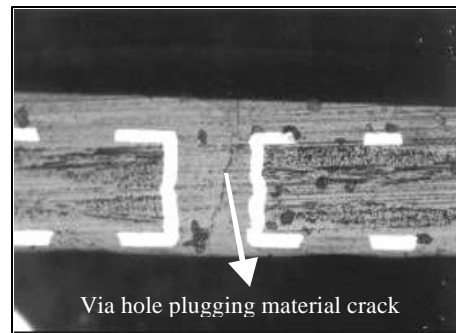


Figure 16. Via hole plugging material crack observed at 1250 cycles

SUMMARY

Underfill adhesion with both chip passivation and solder mask dictates whether underfill delamination finally occurs. Underfill A that has superior adhesion with various interfaces does not show delamination throughout the whole thermal cycle test. Most importantly, no solder bump crack that is the direct reflection of severe CTE mismatch has been detected. On the other hand, solder bump bridging and especially underfill crack do exist and are considered as a potential threat to package reliability. The former defect can be minimized by reducing trapped voids mainly via substrate design as well as assembly

process optimization. Reflowable underfill does not contain silica filler, thus its fracture toughness is lower than proper silica filled epoxy system [5], which can cause underfill crack under the excursion of cyclic stress. Further work on formulation has to be done in order to increase the fracture toughness of reflowable underfill without deterioration of other material properties like wettability, glass transition temperature, flexural modulus and material processability etc. Furthermore, reflowable underfill containing at least 50% silica coupled with the methodology to apply that material are believed to be the only solution for higher reliability demanding. On the whole, flip chip package with 10mm x 10mm chips and being assembled with reflowable underfill without filler (CTE: 70 ~ 90 ppm/°C) enable to survive TCB 1000 cycles. That meets the general requirement for consumer devices.

REFERENCES

- [1] C.P. Wong, S.H. Shi and G. Jefferson, "High Performance Low-cost Underfills for Flip-Chip Applications", IEEE 47th ECTC Proceedings, San Diego, CA, 1997
- [2] Tie Wang, P. Miao, J. Kee and C. Lin, "Wettability Studies of A Reflowable Underfill", 5th Annual Pan Pacific Microelectronics Symposium, Maui, Hawaii, 2000
- [3] Tie Wang, C. Lum, J. Kee, T.H. Chew, P. Miao, L. Foo and C. Lin, "Studies on A Reflowable Underfill for Flip Chip Application", IEEE 50th ECTC Proceedings, Las Vegas, NE, 2000
- [4] A.E. Lucero, R. Dias and T. Pavey, "Predictive Reliability Modeling for Flip chip Interconnect Bump Extrusion", IEEE 50th ECTC Proceedings, Las Vegas, NE, 2000
- [5] X. Dai, M.V. Brillhart, M. Roesch and P. S. Ho, "Adhesion and Toughening Mechanisms at Underfill Interfaces for Flip-Chip-on-Organic-Substrate Packaging", IEEE Transactions on Components and Packaging Technology, Vol. 23, No.1, March 2000