

Flip Chip on Lead-Frame Assembly Using Copper Pillar Bump Technology

There is an increasing awareness of lead pollution throughout the world due to environmental concerns. Semi-conductor companies in the European Union (EU) have agreed to reduce the lead content in all components and assemblies to 0.2% by weight by January 2006. Other countries are already passing similar legislation and most plan to closely follow the EU timeline for lead elimination.

Various lead-free compositions have been put forward; Sn/Ag; Sn/Ag/Cu; Sn/Bi; Sn etc., as replacement for lead. Each metallurgy has its own benefits in terms of cost, reliability, yield, environmental impact and processability. There is no clear material of choice for lead-free packaging and one of the main difficulties is finding one solution that meets the reliability requirements for all industry applications.

Advanpack Solutions' has developed a very robust and wide ranging lead-free interconnect technologies for flip chip attachment of silicon die to a variety of different substrate material. The interconnect technology developed by APS uses a copper pillar capped with a solder. The solder can be either eutectic tin/lead (Sn/Pb) or a pure tin solder that can be reflowed in standard reflow ovens available in the assembly market. Although the eutectic solder composition of 63Sn/37Pb contains lead, in most cases the amount of lead is less than 0.2% by weight, which still complies with the JEDEC definition of a lead-free component. However, if a true 100% lead-free version is required APS has demonstrated that the copper pillar bump with a pure tin solder is a reliable solution and it has been shown to actually improve thermal fatigue life.

The Copper Pillar Bump structure, shown in Figure 1, reduces the amount of solder required to form a good electrical interconnect. In a normal 100% solder interconnect, the solder serves as the support structure, electrical conductor, and the mechanical wetting agent to the substrate and die. APS Copper Pillar Bump replaces a majority of this solder with copper and minimizes the amount of solder required. The elongated copper portion then takes on the function of structural support, interconnect to the die pad, and electrical conductor. The solder cap on the tip of the copper serves mainly as a mechanical attachment of the copper pillar to the substrate.

This report shall detail the flip chip assembly process used to build a 100% lead-free Quad Flat No Lead (QFN) package and the reliability of the QFN package. The packages studied were assembled using the APS' Copper Pillar Bump technology with a pure tin solder cap and were assembled on bare copper lead-frames using both standard mold compound and "green" mold compound. The assembled packages were subjected to very stringent reliability testing including Moisture Level Pre-condition at Level 1 (85% RH at 85°C), and Temperature Cycle B (-55°C to 125°C) in addition to High Temperature Storage Test (150°C) for 1000 hours. In all cases the Copper Pillar Bump was shown to be easy to assemble while meeting all of the most stringent reliability requirements commonly used today.

Simplified Assembly Process Using Copper Pillar Bump Technology

The Copper Pillar Bump structure consists of a reflow-able solder tip on a non-reflow-able copper pillar as shown in Figure 1. In most cases the elongated copper portion is manufactured with a height of 60-70 μm . The height of the Copper Pillar structure is important in maintaining a consistent gap between the die and lead-frame and the amount of solder placed at the tip of the Pillar is also important in forming a good solder connection and high yielding process. It has been found thru this and other testing that the amount of solder on the tip should be between 20 to 35 μm in height in order to give a high yielding and robust assembly process and the highest reliability. It should be noted that too much solder is also not desirable and could lead to other defects like solder bridging or solder spreading on the lead-frame.

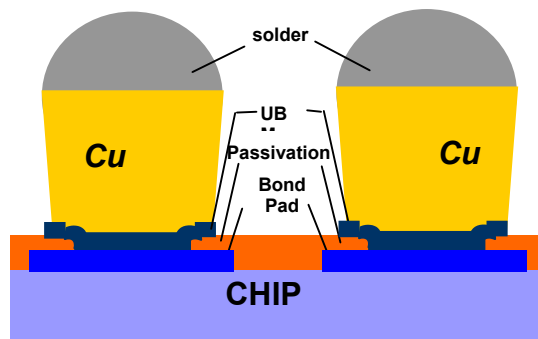


Figure 1: Copper Pillar Bump On Die

Using copper pillar bump to assemble flip chip on leadframe is a relatively simple process when compared with screen print processes commonly used today. The screen print method requires (Reference US 6,482,680 patent, title “Flip-Chip On Leadframe.) solder paste to be deposited onto the lead-frame either through dispensing or screen printing. The bumped chip is then positioned onto the solder paste and sent through a reflow oven to make solder joints on the lead-frame. The IC device is usually bumped with a high lead solder, which normally has a higher reflow temperature than the solder paste. This combination of solder paste with the high lead bump allows the solder paste to reflow with secondary reflow of the bump. Usually screen-printing requires cleaning after reflow since a large amount of flux is used in solder paste printing. In addition to the extra cleaning step, solder paste printing is more expensive and it is quite difficult to get a consistent shape and good positional accuracy of the deposit.

The APS attachment method is much simpler and cheaper than the screen print flip chip attachment process. For the Copper Pillar bump process, once the wafer has been bumped and sawn into individual die, the pillar bumped die is simply picked up and dipped into a small amount of flux and then positioned onto the bare leadframe. No secondary solder or solder paste is required to form a good bond between the bump and lead-frame. The lead-frame used in this study is bare copper (Cu 194) but other copper alloys have been used successfully without issue. After the die is mounted onto the lead-frame, the lead-frame and die sub-assembly are passed through a standard reflow oven. During reflow the flux is activated and the solder is melted to allow it to wet to the surface of the lead-frame. A no-clean flux is used so cleaning is not required after the reflow cycle. Once the solder cools a bond is formed between the die and lead-frame and the flip chip attach process is complete. Figure 2 shows a cross-sectional diagram of the final Pillar Bump and lead-frame sub-assembly after the reflow process.

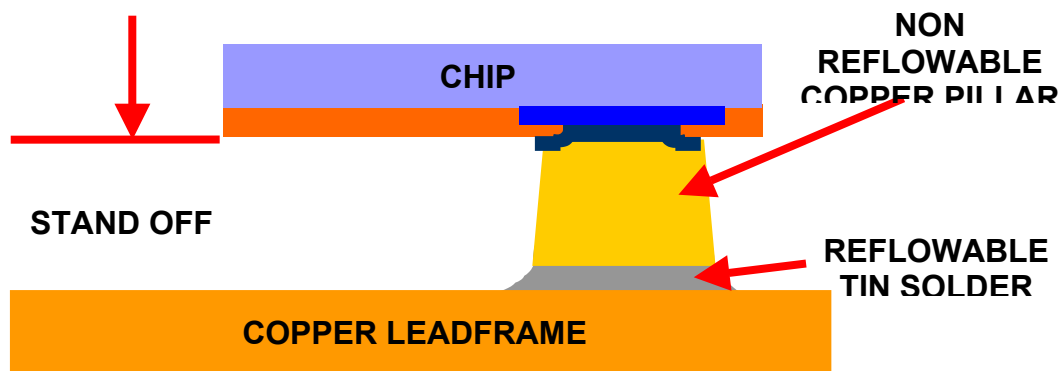


Figure 2: Cross-Section Diagram of Copper Pillar and Lead-frame

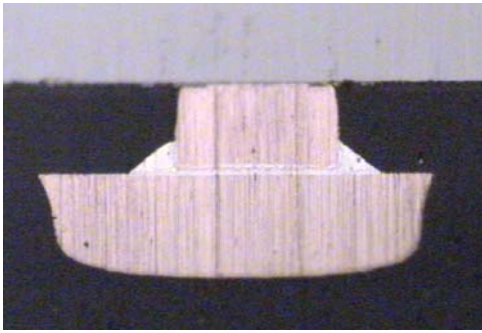


Figure 3

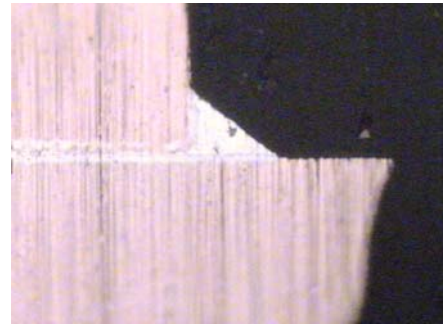


Figure 4

Figure 3 and Figure 4 show the cross-sectional view of the actual assembled units.

Die shear test was conducted on the sub-assembled unit after reflow. This is a destructive test. The average shear reading per bump is $11.2\text{mg}/\mu\text{m}^2$ compared to the minimum specification requirement of $3.2\text{mg}/\mu\text{m}^2$ used for eutectic solder. The failure mode of the shear test is at the tin solder, and which we usually termed as cohesive failure. Figure 5 and Figure 6 show the failure mode on the leads and on the pillar bump respectively.

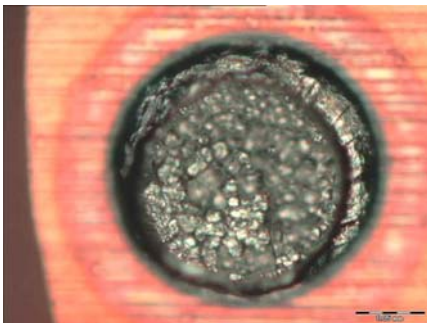


Figure 5
Remains on the Leadframe



Figure 6
Remains on the copper pillar

The rest of the sub-assembled parts were assembled as per normal downstream process (mold to singulation).

Reliability Data

77 units each of QFN 5X5 assemble were subjected to Moisture Sensitivity Level 1 test (85%RH/85°C for 168 hours) and 3X reflow at 260°C peak temperature. The pre-conditioned samples were electrical tested, visual inspected under 40X magnification and sample SAM. After the pre-condition, the samples were subjected to temperature cycles condition B (-55°C to +125°C).

Note: Extra units were inserted into the test for x-sectioning purpose.

Hot Temperature Storage Test up to 1000 hours at 150°C was conducted on 45 units each mold compound type.

Results of the test as per attached. At the time of writing, there are still no failures at the temperature cycles.

QFN PACKAGE (mm)	5X5	5X5
Lead Count	32	32
Die Size (mm)	3.97 x 3.97	3.97 x 3.97
No. of Bumps	28	28
Leadframe Type	Copper	Copper
Mold Compound	Sumitomo MC	Sumitomo Green MC
Moisture Sensitivity Level	1	1
Reflow	3 x 260°C	3 x 260°C
Results	0/77	0/77
Temperature Cycles (B)		
1000 cycles	0/77	0/77
2000 cycles	0/77	0/77
3000 cycles	0/77	0/77
4000 cycles	0/77	0/77
5000 cycles	0/77	0/77
HTST	150°C	
500 hours	0/45	0/45
1000 hours	0/45	0/45

Table A
Reliability Data. Temperature Cycles and HTST

Units were taken out at various temperature cycles interval for crossed sectioning for intermetallic formation inspection. For Hot Temperature Storage Test, sample units were taken out at 1000 hours for crossed sectioned to view the intermetallic formation and other visual defects.

Cross Sectioned Analysis for the Temperature Cycle Parts

3 distinct layers can be observed in the crossed sectioning of the temperature cycles parts. The first layer nearest to the copper pillar and the copper leadframe is Sn and Cu intermetallic layer (rich in Cu), the second layer is another Sn and Cu intermetallic layer and the third layer (center) is Sn layer.

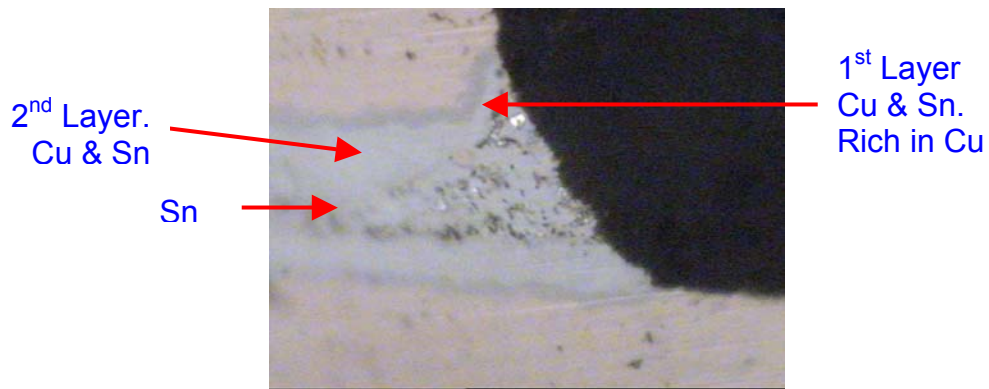


Figure 7
Various intermetallic layers

Attached is the photograph of the crossed sectioned parts, from 0 to 1500 temperature cycles. After 500 temperature cycles, the intermetallic growth started to stabilize.



Figure 8
0 Temperature Cycle

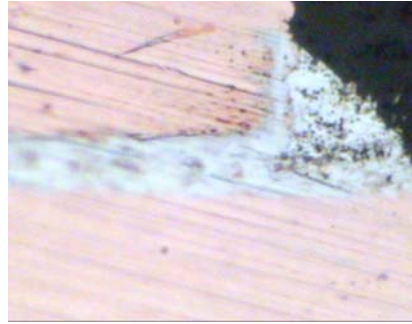


Figure 9
300 Temperature Cycles



Figure 10
500 Temperature Cycle



Figure 11
700 Temperature Cycle



Figure 12
1000 Temperature Cycle



Figure 13
1500 Temperature Cycle



Figure 14
2500 Temperature Cycle



Figure 15
3500 Temperature Cycle



Figure 16
4000 Temperature Cycle

No. of Temp. Cycle	Inter Metallic Layer		
	1st layer Cu & Sn (%)	2nd layer Cu & Sn (%)	Sn (%)
0 Cycles	9.7	37.3	53.0
300 Cycles	13.3	36.3	50.4
500 Cycles	14.6	47.9	37.5
700 Cycles	15.4	43.3	41.3
1000 Cycles	14.3	58.2	27.5
1500 Cycles	14.0	47.7	38.3

Note : Thickness of material in percentage (%) base.

Table B
Intermetallic formation data

Cross Sectioned Analysis for the HTST Parts

The packages were cross sectioned after the 1000 hours. 2 distinct layers can be observed. First layer nearest to the copper pillar and copper leadframe is Cu rich Sn-Cu intermetallic layer and the core layer is Sn-Cu intermetallic layer.

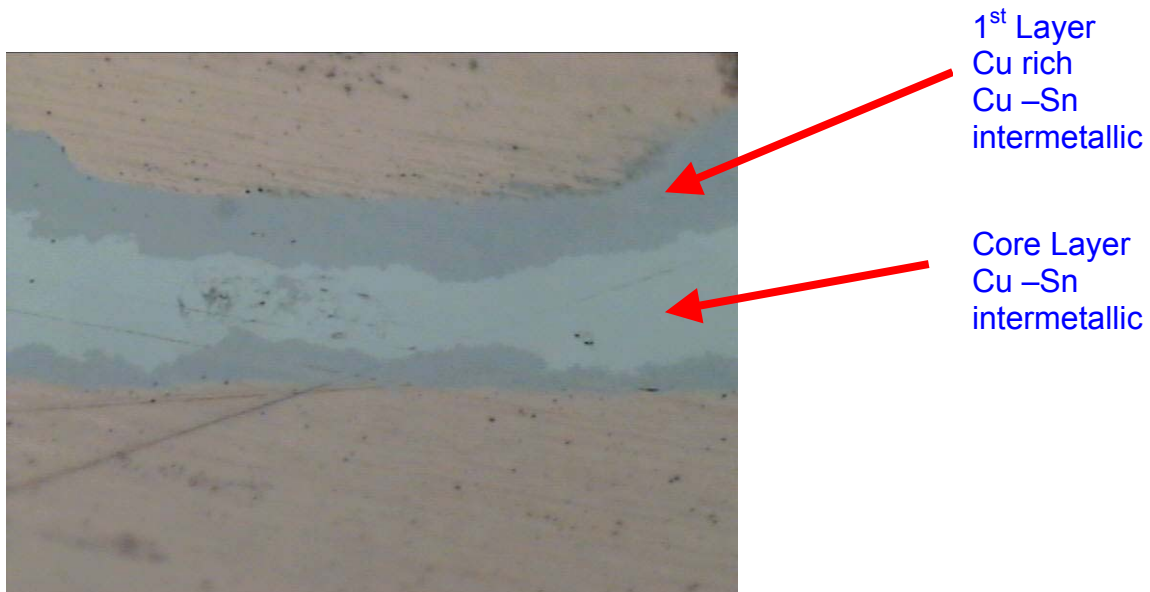


Figure 17
Intermetallic formation at HTST

Kirkendall void can be found on the Hot Temperature Storage Test parts. Refer to the photograph.



Figure 18
Kirkendall void formation at HTST

The impact on the reliability on the 2 type of mold compound (normal and “green”) is minimal. Both mold compounds pass the 1000 temperature cycles with Moisture sensitivity 1 and 1000 hours of Hot Temperature Storage Test.

Conclusion

The flip chip on leadframe process is simplified by using the copper pillar bump technology.

Using pure tin on copper pillar bump for lead-free is a good and viable solution. It has been demonstrated that parts build with such structure can withstand up to 5000 temperature cycle condition B with Moisture Sensitivity 1 and 1000 hours of Hot Temperature Storage Test.

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Acknowledgement

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Reference

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